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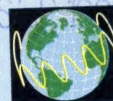
# EDN<sup>®</sup>

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

**Cover Story:**  
**PCs and telephones start to merge** pg 34

AUGUST 3, 1995

26 SEP 1995



Communications  
System Design Issue

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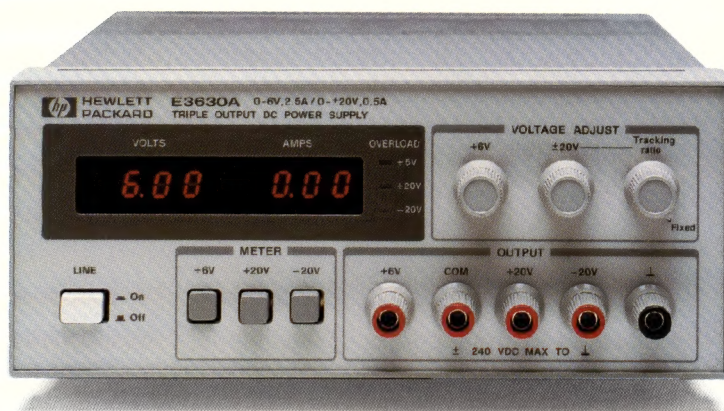


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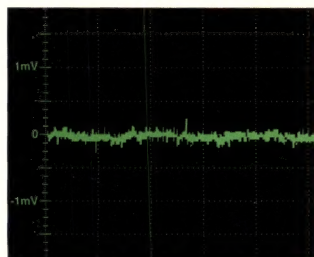
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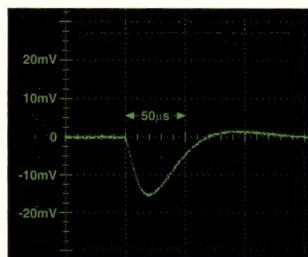
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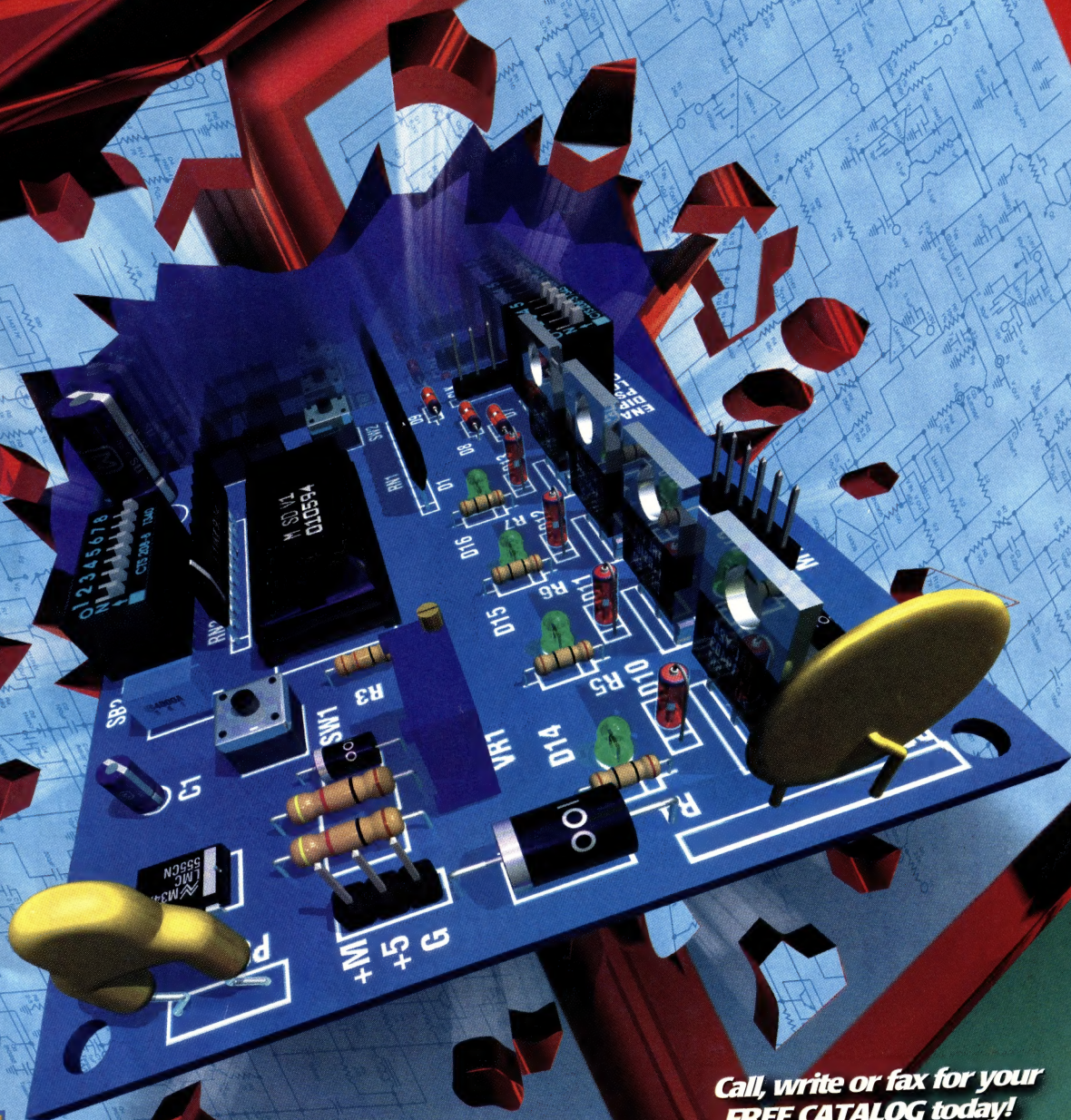
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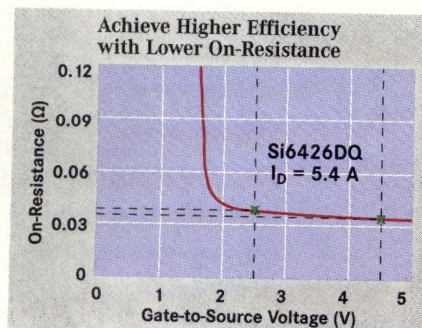
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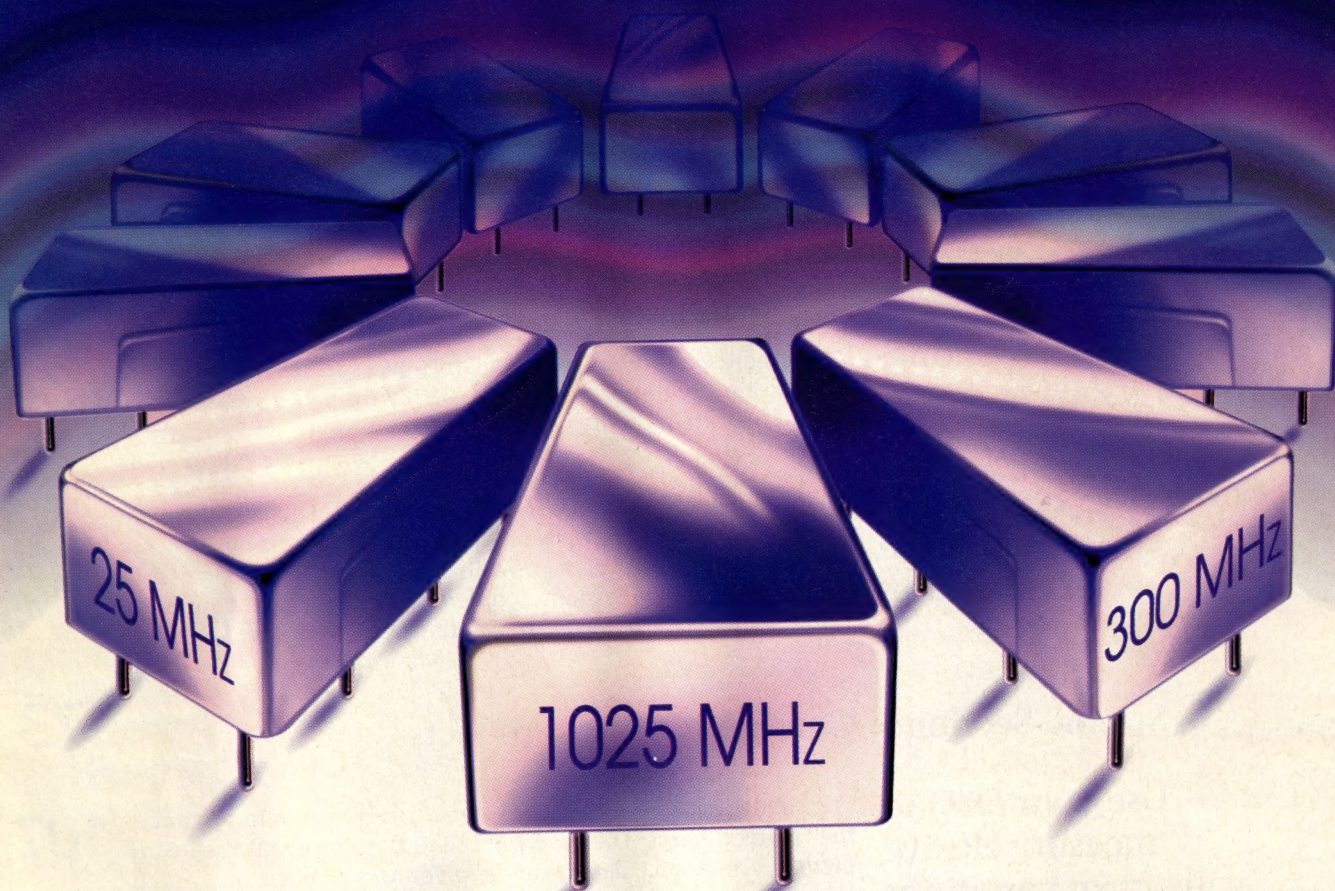
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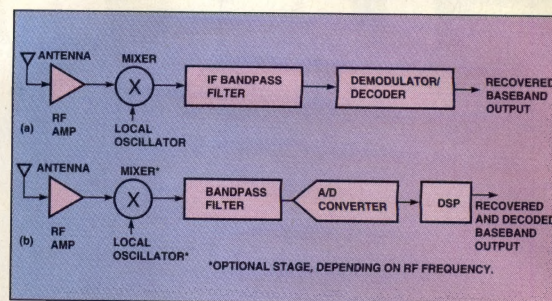




Digital photocomposition by Bryce Flynn/BFP Imaging  
Concept by Richard Quinnell

## PCs and telephones merge

34



## Communication converters

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EDN

## DESIGN FEATURES



## PCs and telephones start to merge

All the hardware and software building blocks are there to turn your PC into a telephone. Those blocks still have rough edges, however, so you have to fit them together carefully.

—Richard A Quinnell, Technical Editor

34

## Converters restructure communication architectures

The superheterodyne-receiver structure has served designers well for more than 70 years. Now, its reign is being challenged by A/D converters, which push digital circuitry closer to the antenna. As a result, you must understand a different set of converter specifications, as well as the hardware trade-offs of a software-based solution.

—Bill Schweber, Technical Editor

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## Special Section: Communications Products

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## Use your DSO to measure elusive waveform variations

The subtleties of how your DSO works can be just as important as the "banner" specs. The time you spend learning about the instrument's performance details can help you to spot waveform anomalies that you never suspected.

—Robert Witte, Hewlett-Packard Co

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## Fixed or floating? a pointed question in DSPs

Designers considering DSP applications must first decide whether to commit their designs to fixed- or floating-point DSPs. The answer may seem to be a trade-off between cost and performance. However, designers must carefully consider a variety of factors before choosing a DSP.

—Jim Larimer and Daniel Chen, Texas Instruments

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## Improved circuit-analysis techniques require minimum algebra

When designing circuits, most analog engineers rely largely on experience and trial-and-error methods, eschewing much of the matrix algebra they learned in college. Using the Extra Element Theorem, however, is a helpful analytical technique that can yield insight into network design.

—Vatché Vorpérian, Jet Propulsion Laboratory, California Institute of Technology

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## Isochronous LAN standard brings real-time video collaboration to the desktop

IEEE-802.9a isoEthernet is the logical choice as the LAN standard of the future. It is interoperable with existing standards. It can provide seamless connectivity over public ISDN networks. And it can isolate local multimedia applications from a company's normal packet LAN/router data flow, thereby maximizing the performance of both local ISDN services and Ethernet packet traffic on the same LAN.

—Rich Brand, National Semiconductor Corp

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## OUT IN FRONT



New FPGA family contains synchronous dual-port RAM **21**  
 BBS is back on line **21**  
 $\mu$ C chip program lets you choose predefined or custom core **21**  
 Customer input refines gang programmer **22**



Dilbert

PCI controller speeds VXIbus beyond embedded-controller rates **24**  
 Signal-processing operating system targets SHARC DSP **26**  
 Plans begin for PCI '96 Week **26**  
 Calendar **26**  
 PCI-to-SCSI host adapters come with a host of features **28**

22 Bandpass filter is most selective monolithic available **28**



CCD sensor for color/black-and-white video measures  $\frac{1}{5}$  in. sq **28**

## EDN

## DESIGN IDEAS

Regulator generates as many as four voltages  
 Data-acquisition system draws less than 10 mW  
 Rotary controller positions stepping motor  
 Circuit loads eight-channel DAC from PC port

89 Resistance calculator yields precise values **98**  
 90 Algorithm evaluates complex fractions **100**  
 92 **EDN** COLUMNIST  
 96 Once upon a time... **191**  
 A fuzzy parable.—David Brubaker, Fuzzy-Logic Contributing Editor

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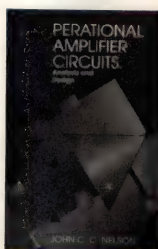
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**EDN****EDITORIAL**

# Repaying a debt



When I started working as an engineer 20 years ago, I knew that I didn't want to work in the defense industry. It wasn't that I fundamentally objected to defense work; it just wasn't right for me. I felt fortunate that enough engineers found defense work interest-

ing, letting me turn my attention to other pursuits. As I write this editorial, Captain Scott O'Grady has just returned from Bosnia, where his plane had been shot down

while patrolling NATO's no-fly zone. He's had lunch at the White House with President Clinton after spending six days eating bugs and grass before his rescue. The story of his crash and escape is one of truly heroic proportions, but O'Grady declines the title of hero. Others deserved it more, he said. Then he went further.

"The greatest gift anyone could ever give me would be if you know anybody [who has served in uni-

form or is serving now] to go up to them and thank them for what they're doing for trying to make this world a better place," said O'Grady.

From my perspective, O'Grady's request applies equally well to the engineering community that has devoted itself to the defense industry. Without its contributions, we would find ourselves in a different world indeed. The O'Gradys of this world would find themselves flying inferior aircraft (or none at all)

and would be shot down with far more regularity. Our nation (and the world) would be a more dangerous place than it is now.

We owe a word of thanks to the design community that has

served us by helping to preserve the peace we enjoy in the United States and in a large part of the world. Currently, these same people are undergoing major trauma as the defense industry shrinks and otherwise adjusts to the end of the Cold War. Their time in the lime-light has passed, for now. However, their mission is no less important than it ever was.

Thank you.

**We owe a word of thanks to the design community that has served us by helping to preserve the peace we enjoy.**

*Steven H. Leibson*

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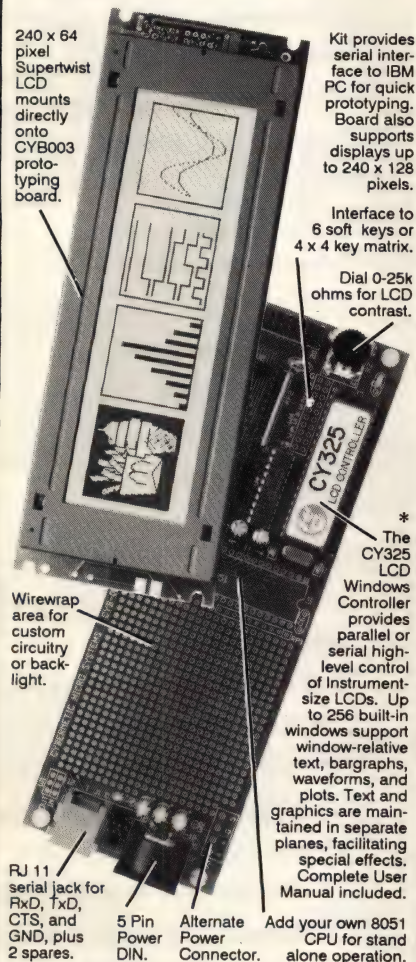
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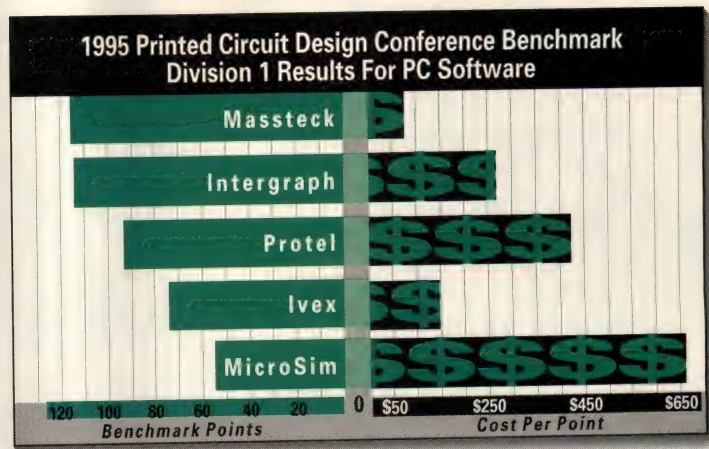
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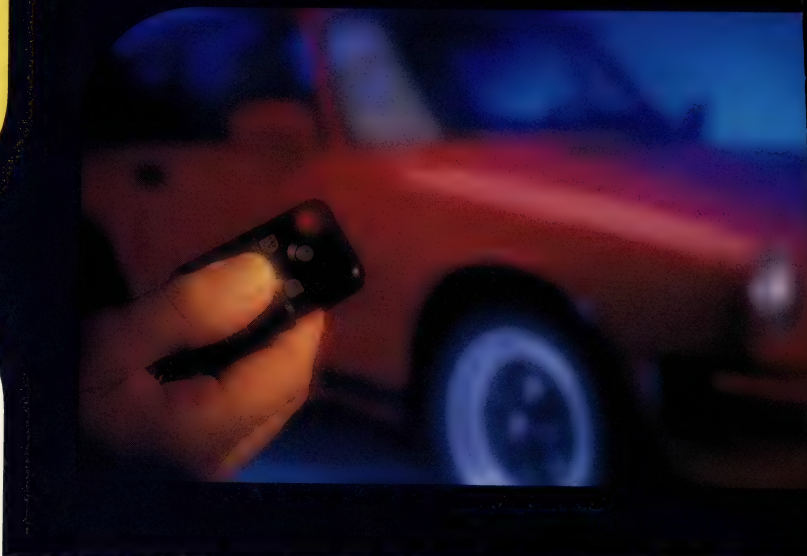
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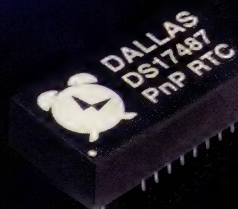


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# It's Plug and Play Time



Looking for a quick and simple way to upgrade your system to Plug and Play? Dallas Semiconductor—the world's leader in computer timekeepers—introduces a family of Plug and Play timekeepers. Each timekeeper comes with extra RAM to store data that tells the computer where all the resource assignments are set. Systems access the timekeeper's extra RAM via software instead of hardware for full Plug and Play capability.

## **Simplest and Cheapest Timekeeping Solution**

- Most systems can be upgraded to Plug and Play simply by changing out the BIOS and the clock. Unlike flash-based solutions, no redesign is required.
- Store the BIOS in One-Time-Programmable (OTP) ROM and use a Dallas clock for the lowest cost Plug and Play timekeeping solution.
- Dallas' Plug and Play solution does not require additional upper memory, thus saving system resources.

## **Increased Flexibility**

- You can store the BIOS in Flash or ROM.
- With the range of memory densities available in the Dallas Plug and Play family, you can design one system that will be adaptable across the gamut from low-end to high-end PCs.

## **Advanced Power Management Features**

- A kickstart input powers on the system with a single keystroke or via a modem ring detect signal.
- A wake-up alarm wakes up the system at a pre-set time; the system then performs its tasks and shuts itself down.
- Our clocks give your system the ability to perform "Soft Power On," complying with the PC '95 Hardware Design Guide recommendation.

## **Unique Extras**

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- Each chip is laser-etched with a guaranteed-unique, 64-bit serial number to help you keep track of your systems.

Device Number	Extended RAM	Operating Voltage
DS1685/DS1687	128 Bytes	3V or 5V
DS17285/DS17287	2K Bytes	3V or 5V
DS17485/DS17487	4K Bytes	3V or 5V
DS17885/DS17887	8K Bytes	3V or 5V

*For more information on the Dallas Semiconductor family of Plug and Play clocks, give us a call at (214) 450-0448.*





# EDN OUT IN FRONT

WHAT'S HOT IN THE DESIGN COMMUNITY

EDITED BY FRAN GRANVILLE

## New FPGA family contains synchronous dual-port RAM

The Xilinx XC4000E family of field-programmable gate arrays (FPGAs) for high-performance applications provides a 50% performance increase over the company's XC4000 FPGAs. The XC4000E offers eight devices ranging from 3000 to 25,000 gates, including the XC4020E device, which is Xilinx's first 20,000-gate device. The XC40003 features on-chip synchronous RAM, reducing chip count and increasing RAM performance by a factor of two; dual-port RAM, enabling on-chip buffering; PCI compliance; and advanced application modules for memory and PCI functions.

The XC4000E architecture is a superset of the XC4000; therefore, the new family is bit-stream-, pin-, and backward-compatible with the XC4000. The speed increase and price reduction stem from the use of deep-submicron, triple-layer-metal technology. Xilinx will manufacture the XC4000E using 0.6- $\mu$ m technology and shrink it to 0.5- $\mu$ m technology in the fourth quarter. The architecture features an enhanced configuration-logic block (CLB) and onboard, synchronous dual-port RAM. The dual-port RAM provides simultaneous read/write functions, and the synchronous RAM allows embedded configuration registers. Taking advantage of three-layer metal, Xilinx redesigned the routing scheme of the XC4000E architecture to improve CLB access and increase connections. The architecture provides shorter wires, which reduce interconnect delays in the devices.

The new architecture also includes the company's application modules (XAMs), pre-engineered functions that simplify and speed system design. XAMs include



The Xilinx XC4000E family has densities of 3000 to 25,000 gates and features on-chip synchronous RAM.

FIFO buffers and PCI building blocks to provide readily available elements that you previously had to purchase as separate components.

You can use the Xact Step software-development system to design with the new XC4000E family. New modules for the Xact Step system allow you to take advantage of the new features of the XC4000E. These modules will be free under maintenance contracts. The XC4005E, which contains 4000 to 5000 gates without RAM and 7000 to 11,000 gates with 10 to 30% RAM usage, is available for sampling now and costs \$105 (100).

—by John Gallant

**Xilinx Inc.**, San Jose, CA. (408) 559-7778.

**Circle No. 485**

**BBS is back on line.** EDN's computer bulletin-board system (BBS) is now back on line after having experienced some technical difficulties. We apologize for the inconvenience. To access the BBS, phone (617) 558-4241 with modem settings 300/1200/2400 8,N,1 (V.32bis (617) 558-4580).

## $\mu$ C chip program lets you choose predefined or custom core

Oki semiconductor has launched a customizable microcontroller ( $\mu$ C)-based chip program that lets you choose a predefined QuickCore  $\mu$ C core or specify a custom-configured core. You then surround the core with your choice of periph-

erals, memory blocks, and user-defined logic to create a customized  $\mu$ C chip.

Two predefined 8-bit cores, the nX 65516 and nX 65524, are available, and the company plans to release 16-bit cores next year. Both of the 8-bit cores operate at 2.7 to 5.5V with a maximum clock speed of 20 MHz. The devices' memory configurations differ, however. If you customize your own core, you can

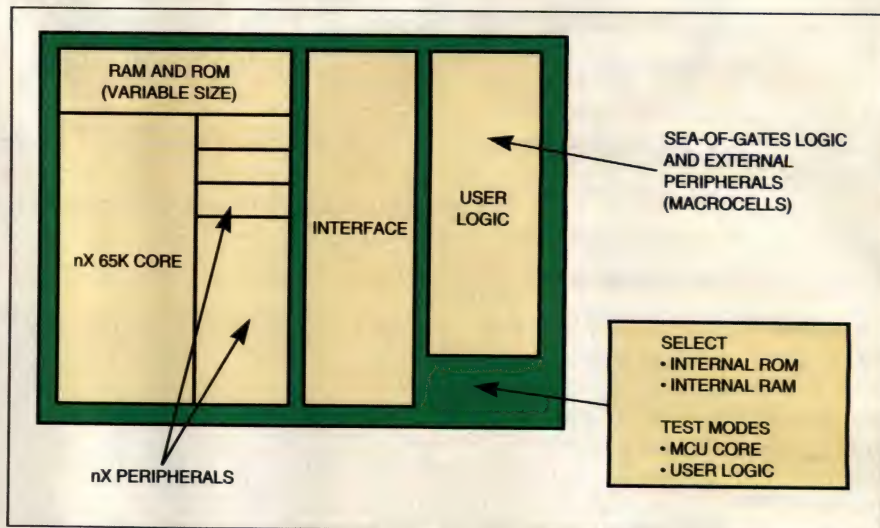
(continued on pg 22)



# EDN OUT IN FRONT

implement up to 64 kbytes of ROM and 16 kbytes of RAM to go with it.

Some of the peripherals you can include with your  $\mu$ C include timers and counters, a multiply/divide unit, UART, an 8-bit A/D converter, an 8-bit shift register, and user-programmable 8-bit I/O ports. You can define as many as 50,000 gates of custom logic in a gate-array design environment using several electronic-design-automation (EDA) tools from Cadence, Mentor Graphics, Synopsys, and Viewlogic. This custom logic can include macrocells from Oki's sea-of-gates library. Oki brings the descriptions of these user-defined blocks into Cascade's Epoch EDA tools; combines the logic with the predefined or customized core; and does the necessary floor-planning, timing simulation, and layout. You then receive a back-annotated netlist comprising a Verilog file, circuit primitives, and a standard-delay-format file for postlayout simulation. On successful simulation, Oki does a final layout verification and fabricates the chip.



**Oki's QuickCore lets you combine a user-configurable 8-bit  $\mu$ C core with predefined macrocells and user-defined logic.**

A test-mode interface isolates user-defined logic from the  $\mu$ C core. This approach simplifies emulation and control of the logic as well as whole-chip emulation and testing. The price of  $\mu$ Cs with QuickCore designs varies, depend-

ing on features and user-defined logic. NRE charges begin at \$100,000 (60,000/year).—by Jim Lipman

**Oki Semiconductor**, Sunnyvale, CA. (408) 720-1900.

**Circle No. 486**

## Customer input refines gang programmer

BP Microsystems' BP-2100 concurrent-programming system is a sophisticated four- to 16-socket gang programmer for memory

and PLDs. The company developed this product from the BP-1200 single-socket programmer for companies with high-volume programming requirements. Essentially, the BP-2100 comprises several BP-1200s in one chassis with memory and

communications hardware. The memory allows each programmer to hold program codes, test vectors, and test results. The BP-1200 stores this data in the host PC. The communications hardware allows several programmers to talk to a PC master system

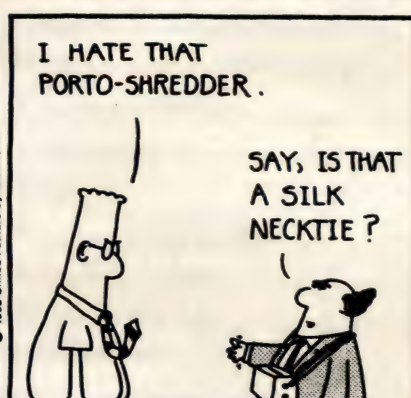
controller, giving the programming system some fault tolerance. If one programmer fails, the rest of the system can still program parts.

Each of the BP-2100's independent programming sockets can have

(continued on pg 24)

## DILBERT® by Scott Adams

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either 84 or 240 pins. The company originally offered only 84-pin programming sockets, but electronics-distributor Wyle Labs, an early customer for the programmer, needed additional programming pins to program complex PLDs. Similarly, Arrow Electronics, another distributor and early customer, requested a change to the programmer's user interface. The programmer now automatically senses when you insert and extract the device to be programmed. It starts programming as soon as you insert the device, lights an LED

when the programming finishes, and extinguishes the LED when you remove the device from the programming socket. Automatic sensing speeds the programming cycle because you do not have to push a start button. Automatic sensing also prevents unprogrammed devices from being mistaken for programmed ones because the LED is off whenever an unprogrammed device is in the socket.

Although the BP-2100's programming sockets are independent, all sockets are set up for the same device, programming

codes, and test vectors. Socket independence allows you to load and unload devices from some of the sockets while the other sockets are programming parts. This feature boosts the programmer's throughput.

In addition to fault tolerance, this design approach allowed the company to reuse all of the BP-1200 programming algorithms. The BP-2100 can program almost 8000 device types, including memories and PLDs. Currently, the programming system cannot program field-programmable gate arrays based on antifuse

technology from Actel, Cypress Semiconductor, and Texas Instruments. BP plans to add support for these devices by the first of October.

Six-socket versions of the BP-2100 with 84 and 240 pins per socket cost \$28,000 and \$35,000, respectively; 16-socket versions with 84 and 240 pins per socket cost \$68,000 and \$85,000, respectively. The company also plans to offer a single-socket version of the BP-2100.

—by Steven H Leibson  
**BP Microsystems,**  
Houston, TX. (713) 688-4600. **Circle No.487**

## PCI controller speeds VXIbus beyond embedded-controller rates

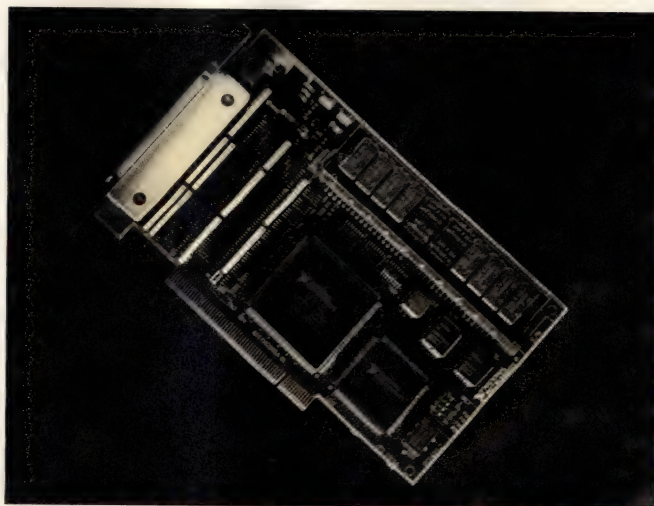
You no longer need an embedded controller to make VXIbus-based modular-instrument systems achieve the highest possible data-transfer rates. National Instruments' VXI-PCI8010 kit allows a sustained transfer rate of 23 Mbytes/sec and burst rates exceeding 33 Mbytes/sec. The kit implements the MXI-2 version of the Multisystem Extension Interface (MXI) bus the company introduced in 1989. The kit includes a PCI-MXI-2 PCI bus plug-in board for the PC, a 2m-long MXI-2 cable, a VXI-MXI-2 board that plugs into the VXI backplane, and NI-VXI and VXIplug&play software for Windows 3.1 and DOS.

Until the advent of MXI-2, embedded controllers, which plug into VXI backplanes, offered the highest transfer rates. The controllers present a few problems, however. For example, they cost more than conventionally packaged desktop PCs of equal performance. In addition, the controllers often don't accommodate the options you can add to standard PCs, and their technology generally lags behind that of desktop PCs by about six

months. For those reasons, many system integrators prefer to use external PCs as controllers. The MXI bus has become an industry standard for connecting those PCs to VXI chassis. The MXI-2 standard is backward-compatible with the original MXI and meets the specifications of the VXIplug&play Systems Alliance.

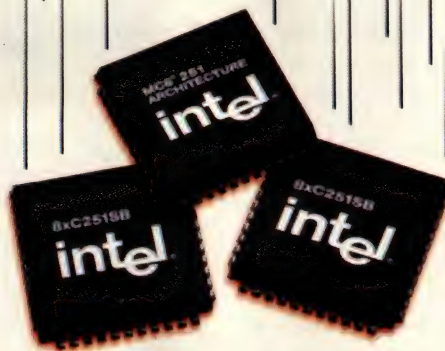
The new product addresses all of the embedded-controller problems, except cost. When you add the \$4100 base price of the VXI-PCI8010 to the cost of a PCI bus-based PC, the price nears that of an embedded controller. On the other hand, the new product's continuous data-transfer rate is more than twice that of an embedded controller. Moreover, you can order both the PCI-MXI-2 and VXI-MXI-2 boards with standard DRAM SIMMs. You can then place up to 64 Mbytes of

dual-ported DRAM on the PCI-MXI-2. This RAM can function either as shared memory or as a dedicated buffer for real-time or post-acquisition data analysis.—by Dan Strassberg  
**National Instruments Corp,** Austin, TX. (512) 794-0100. **Circle No. 488**



**The National Instruments PCI bus-based controller for the MXI-2 bus, an updated version of the industry-standard MXI bus, offers high-speed data transfers between external PCs and the VXIbus.**





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## Signal-processing operating system targets SHARC DSP

Spectron Microsystems has ported its Spox 2.0 operating system to Analog Devices' flagship ADSP-2106x SHARC DSP and to the ADSP-2102x of DSPs. The availability of the widely used Spox environment allows mainstream developers to take advantage of the 120-Mflops SHARC, which Analog Devices claims to be the highest performance single-processor DSP available. The port includes the compact Spox kernel and Spectron's suite of signal-processing software-development tools that support applications ranging from multimedia PCs to instrumentation to telecommunications.

Spox will accelerate SHARC-based developments by providing designers a software base for applications. The software provides real-time multitasking services, inter-processor communications capabilities, device drivers, and bridges to other operating systems, including DOS, Unix, VxWorks, and OS/9. The Spox 2.0 application interface includes queues, semaphores, mailboxes, streaming I/O, and other real-time features to meet programmer requirements.

Due to its modular architecture, Spox suits applications from miniature embedded systems, such as portable communication devices, to reprogrammable desktop multimedia systems. Moreover, you can easily apply the device-independent I/O structure and task-service facilities to the multi-processing applications that the SHARC DSP architecture targets.

Spox 2.0 for the ADSP-2106x and ADSP-2102x families costs \$12,000 and includes development and runtime licenses. Production releases of the kernel and the Spox-Link host-communications library are available now. Other Spox components, including a debugger and math library, will be available during the fourth quarter. This year, SPOX 2.0 will also be available preported to ADSP-210xx boards from multiple vendors, including Ariel, Ixthos, and Loughborough Sound Images.—by Maury Wright

**Spectron Microsystems Inc.**, Santa Barbara, CA. (805) 968-5100.

**Circle No. 489**

## PLANS BEGIN FOR PCI '96 WEEK

Though the last PCI Week has just ended, preparations are under way for next year's conference, which will take place at the Red Lion Inn in San Jose, CA, on April 29 to May 3, 1996. Organizers are soliciting proposals for papers on design-related topics, such as electrical or mechanical bus design, ICs and other semiconductors for the Peripheral Component Interconnect (PCI) bus, PLDs applied to PCI design, software design, embedded PCI applications, and alternative PCI form factors. Slots are also open for half- and full-day tutorials. Tutorial presenters receive payment for their participation in the conference. Send your proposals to: Dr Lance Leventhal, Annabooks, 11838 Bernardo Plaza Court, Suite 102A, San Diego, CA 92128-2417. (800) 462-1042 or (619) 673-0870; fax (619) 673-1432.

## CALENDAR OF UPCOMING EVENTS . . .

### Aug 13 to 17

**Object World**, San Francisco, features more than 48 sessions on applying object technology. The event features 19 tutorials and more than 100 exhibitors. Object World Expo, Framingham, MA. (800) 225-4698.

### Aug 17 to 20

**The California Computer Expo**, San Diego, combines more than 400 exhibits and 230 seminars with hands-on instruction. Topics include virtual reality, the Internet, and business computing. The California Computer Expo, San Diego, CA. (619) 573-0617.

### Aug 27 to 31

**Surface Mount International**, San Jose, CA, is a conference and exhibition covering emerging electronics-manufacturing technologies. The program features sessions on ball-grid arrays, chip-scale packaging, PC-Cards, and component technology. Sponsors are the Electronic Industries Association, Arlington, VA (703) 907-7500; The Institute for Interconnecting and Packaging Electronic Circuits, Lincolnwood, IL (708) 677-2850; Miller Freeman Inc, San Francisco, CA (415) 905-4994; and the Surface Mount Technology Association, Edina, MN (612) 920-7682.

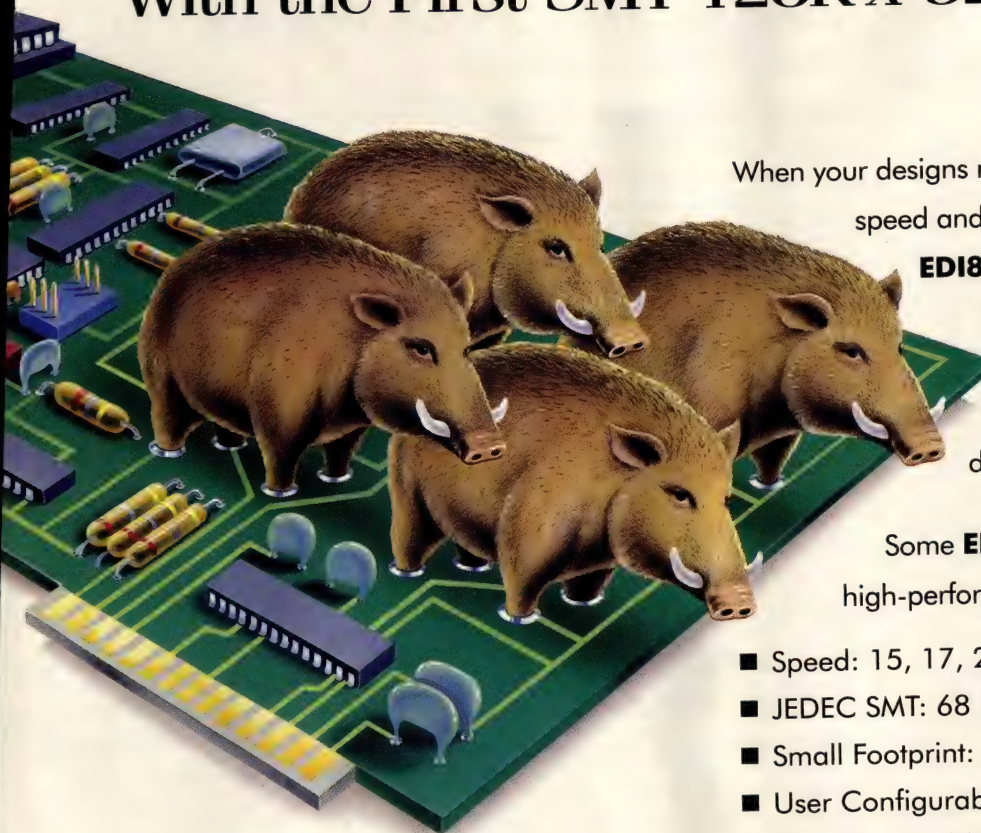
### Sept 14 to 15

**Embedded Systems Conference**, San Jose, CA. This event for software developers and engineers involved in embedded design combines the largest exhibition of products and services with lectures and tutorials. Miller Freeman Inc, San Francisco. (415) 905-2354.



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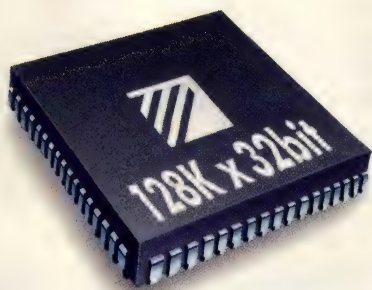
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**Linear Technology Corp**, Milpitas, CA. (800) 454-6327.

**Circle No. 491**

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Available in four models for color or black-and-white use, US and European standards, Sony's  $1/5$ -in.-sq (5-mm-sq) CCD sensors suit consumer and commercial security, PC-video-conferencing, and image-recognition applications. The devices feature 360- to 210-mV/lux-sec sensitivity and 362 $\times$ 492- to 358 $\times$ 583-pixel resolution. The ICX076AL, ICX077AL, ICX076AK, and

ICX077AK video sensors come in 14-pin plastic packages.

All devices offer low dark-current and low smear characteristics and high antiblooming performance. Sony achieves the high sensitivity and low dark current through use of hole-accumulation diode sensors in the devices' fabrication. System frequency is 13.5 MHz; the horizontal register and reset gate use 5V drive. Prices are \$45 (samples) and \$19 (10,000).—by Bill Schweber

**Sony Semiconductor Co of America**, San Jose, CA. (800) 288-7669.

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ing, Power Integrations Inc.

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1990 - PWR SMP-3  
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1992 - ADXL50

Acceleration Sensor,  
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1993 - LTC1145 and LTC1146 Isolator ICs,  
Linear Technology Corp.

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1990 - Crosscheck Test Technology,  
Crosscheck Technology Inc.

1991 - HP54600A 100-MHz Digital Storage  
Oscilloscope, Hewlett-Packard Co.

1992 - 90-Series Scopometers, John Fluke Mfg  
Co Inc./Philips Test and Measurement

1993 - TDS 544A Digitizing Oscilloscope,  
Tektronix Inc.

### CAE/CAD

1990 - Analog Fasttrack design system,  
Harris Semiconductor

1991 - Falcon Framework For Concurrent  
Design, Mentor Graphics Corp.

1992 - DESP Station Software,  
Mentor Graphics Corp.

1993 - Analog Model Synthesis, Analog Inc.

### Computers and Peripherals

1990 - Hp 48SX scientific calculator,  
Hewlett-Packard

1991 - Color LCD Technology,  
In Focus Systems Inc.

1992 - Stingray 1842 1.8-in. Disk Drive,  
Integral Peripherals Inc.

1993 - Touchmate Touch-Sensing Peripherals,  
Visage Inc.

### Components, Hardware and Interconnects

1990 - EL 1C-C000 VGA display, Cherry Corp.

1991 - Isocon Interconnection System,  
Rogers Corp.

1992 - AX1024 Programmable Interconnect  
Device, Aptix Corp.

1993 - Cro-Bar Electrostatic-Discharge  
Protective Device, Polaroid Corp.

### Software

1990 - Tekcolor CMS, Tektronix Inc.

1991 - IRMX For Windows, Intel Corp.

1992 - Gabor Spectrogram,  
National Instruments

1993 - Visual C++ Development System For  
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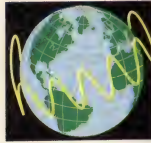
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# PCs AND TELEPHONES START TO MERGE







## RICHARD A QUINNELL, TECHNICAL EDITOR

Since the PC has appeared on our desktops, it has slowly absorbed virtually everything else that used to reside there: notepads, business-card files, address books, and drawing tools. Soon, it will absorb the telephone. That integration of computer and telephone opens the door to a host of telephone-enabled applications. Getting the pieces to fit together is the challenge.

The term "computer telephony" (CT) implies different things to different people. Their visions range from separate but coordinated telephone and database networks to the desktop computer as a combination speaker phone and answering machine (see **box**, "Computer telephony's many extensions"). Regardless of how they define CT, however, people in the communications industry agree that these two information-handling technologies are merging.

The current growth in CT began with the release of foundation software by computer-industry leaders Intel, Microsoft, and Novell. Novell, which dominates the PC-networking market, created a telephony-services application-programming interface (TSAPI) for the NetWare operating system. The TSAPI links the network's capabilities to those of the private-branch-exchange (PBX) switch. Intel and Microsoft, which dominate the PC's architecture and operating system, jointly created a telephony application-programming interface (TAPI) that gives Windows programs control over telephone call-handling functions. Both interfaces insulate application programmers from the details of the telephone system in use, eliminating the need to adapt programs to dozens of phone systems. The unified programming environment provides fertile ground for a range of CT applications to take root.

### Architecture links PCs and phones

If you're growing your own CT application, one of the first things you need to consider is the archi-

tecture that connects the computer to the telephone. Three basic architectural structures have evolved, each with its advantages and limitations. The PC can link to the PBX through its network server (**Fig 1a**). Alternatively, the PC can tie directly to the telephone (**Fig 1b**), or the PC can serve as the telephone itself (**Fig 1c**).

Linking the PC and telephone through the network server involves the smallest hardware cost for larger installations. The only special hardware this

architecture requires is the link between the server and the PBX; all other computers on the network need only telephony software. The PBX supplies the network with call-control information, such as caller ID, and the network uses the PBX to direct and manipulate calls.

This architecture has been in use for several years. Until the advent of TSAPI, however, application programmers had to rewrite programs for each of the more than 40 PBX switches on the market. Such rewriting was difficult, if not impossible, because PBX manufacturers kept their

systems proprietary. Now, however, most PBX manufacturers supply TSAPI drivers, so that application programs can run unchanged on a variety of machines.

Computers running Windows TAPI-based applications can also run with this architecture by using the Tmap software, which Northern Telecom developed. TAPI links applications to hardware through the TAPI service-provider interface (TSPI) (**Fig 2**). Tmap makes the TSAPI network look like a service provider to TAPI and translates TAPI commands to TSAPI commands.

The disadvantage of connecting the PC and telephone networks through the PBX is that the PCs don't gain access to the voice information, only the call-control data. A way around this limitation is to bring telephone lines to the server. By incorporating telephone cards such as those from Dialogic and others (**Table 1**), the server can act as a telephone, providing a path for network-stored outgo-

**All the hardware and software building blocks are there to turn your PC into a telephone. Those blocks still have rough edges, however, so you have to fit them together carefully.**



## COMPUTER TELEPHONY

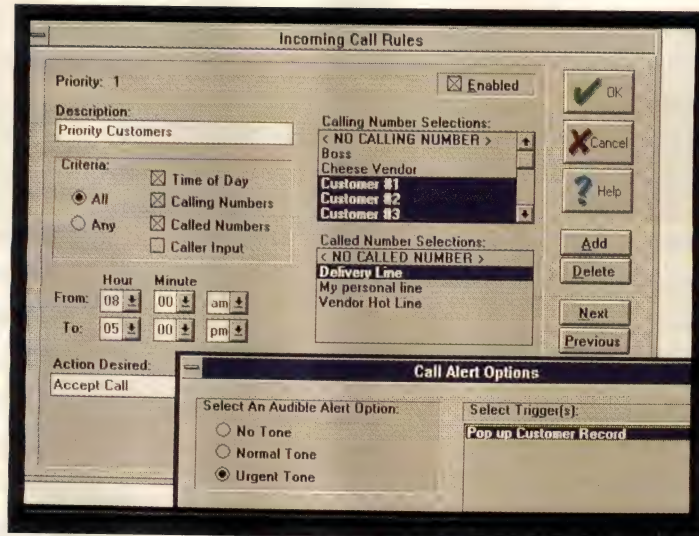
ing messages and for answering-machine functions. These telephony servers also provide an opportunity to add computation-intensive functions, such as speech recognition, to the system by tying powerful DSP boards to the telephone interface.

### PC-to-phone link

Directly connecting the PC to the telephone unit, the second common architecture may or may not provide the PC with access to the voice data. At the very least, however, this architecture provides computer control over the telephone in use as well as access to caller-ID and other call-setup information. The computer can then serve as a graphical interface for the telephone system's advanced functions, such as conference calling, and make intelligent decisions about where to forward incoming calls. The com-

puter can also dial calls using information from user programs, such as address books, or can provide "screen pops," which are database displays specific to an incoming call.

Such direct connections typically use an adapter or a modified phone unit with a data link to a PC. C-T Link's recently introduced C-T Link 1000A,

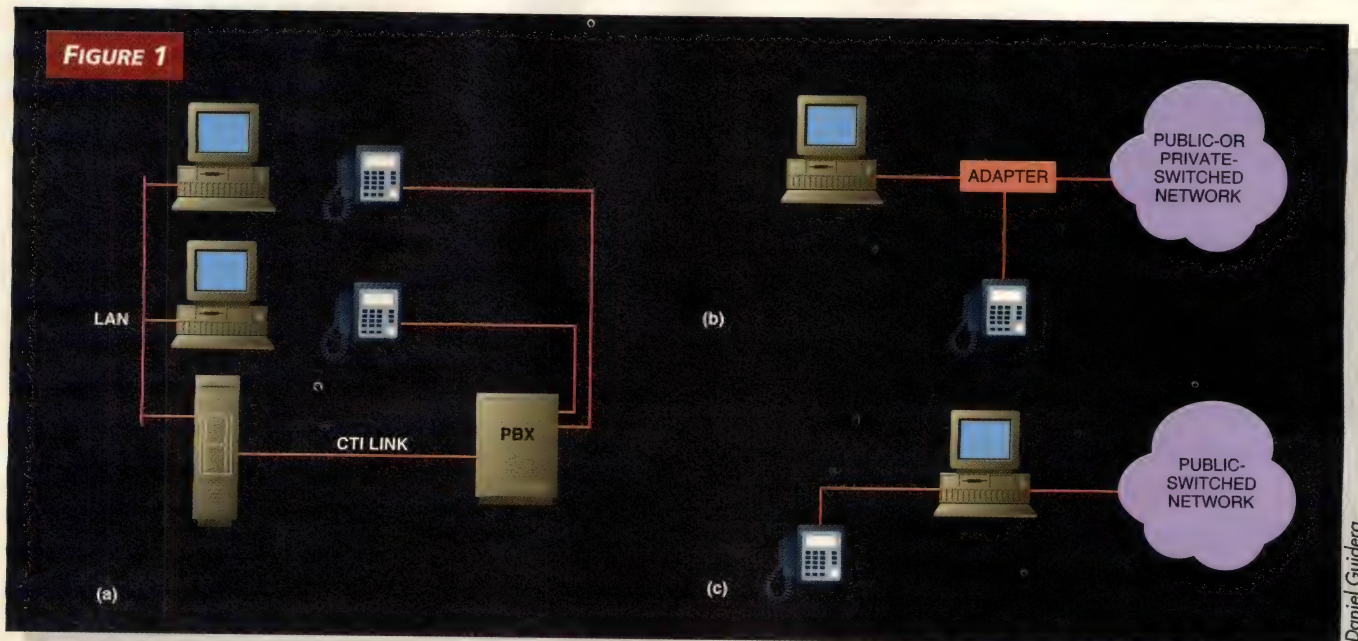


**Middleware, like Aurora's FastCall, allows you to build applications without programming. By defining a set of rules, you customize the middleware into an application program that meets your needs.**

for example, connects with the standard telephone network. This device shares the PC's parallel port with the printer to provide a control link to a standard analog telephone. The control link allows Windows applications to place calls and to receive caller IDs. Future product generations will use the high-speed Universal Serial Bus (USB) for peripherals. Several companies, including Intel, Microsoft, and Compaq, are developing USB, which will allow digital-audio and control data to pass between the PC and the telephone line.

### PC becomes the phone

The third architecture resembles the traditional data-communications structure, in which the PC connects directly to the telephone network and offers an optional pass-through to a telephone handset. With the proper interface circuits, this configuration works with any telephone system, including analog, ISDN (integrated services digital network), and digital PBX. Because embedded-



**How a computer interacts with a telephone depends on the connection architecture. With a host-to-switch link (a), the telephone and computer are logically paired without a direct connection. The PC can hook to the phone handset (b) for more direct control or connect to the network directly (c) to act as a telephone itself.**



system designers will most likely adopt this configuration when adding telephony functions to their systems, this approach merits closer examination.

Fig 3 details the hardware needs of such a computer telephone connecting to the public-switched telephone network (PSTN). The computer telephone's main elements are the data-access-arrangement (DAA) circuit, the data pump, a microcontroller, and the PC interface, each of which has many variations. There must also be an audio interface to allow the system to provide the voice functions.

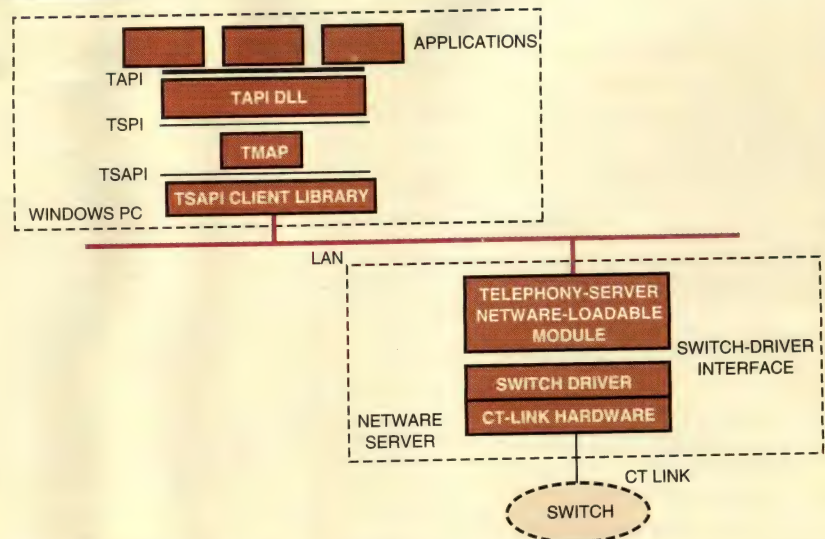
The DAA circuit provides the final connection between the computer and the telephone network. Depending on the network in use, the DAA may provide an analog interface to the PSTN, use a digital interface to a PBX or to the ISDN, or connect to a cellular transmitter. This interface also varies within each of these categories. Connection to PBX switches, for instance, varies with the switch manufacturer. The PSTN interface differs for each country in which the DAA circuit must operate.

The data pump handles the conversion between digital information and audio tones. It also produces and decodes dual-tone multifrequency (DTMF) tones, provides line equalization, and performs echo canceling. A data pump typically comprises a DSP and either an analog front end or a codec for A/D and D/A conversion. A data pump can also be a simple analog codec that combines with the inherent processing power of the host PC, as with Intel's Native Signal Processing.

The microcontroller formats the data for audio encoding, including bit scrambling to break up long repeating strings, addition of error-correction codes, and data compression. It also reformats serial incoming data and provides the interface to the PC bus. This control function might use a separate microcontroller, be integrated into the data pump's DSP, or be handled by the host processor.

High-speed modem chip sets for fax and data communications include all of these functions. To be suitable for telephony, however, the modem must also offer a voice path. As Fig 3 shows, the voice path requires an additional

**FIGURE 2**



Tmap software acts as a service provider to TAPI and looks like a client to TSAPI, seamlessly bridging the two telephony approaches.

**TABLE 1—REPRESENTATIVE COMPUTER-TELEPHONY MANUFACTURERS**

Product Type	Manufacturers
<b>Algorithm vendors</b>	DSP Software Engineering GAO Research & Consulting HotHaus Technologies VoCal Technologies
<b>Application software</b>	Active Voice Applied Voice Technology Delrina Phoenix Technologies Radish Communications Systems
<b>DSP tools and libraries</b>	Analogic Corp Spectron Microsystems Spectrum Signal Processing
<b>DSP/data-pump chips</b>	Analog Devices AT&T Microelectronics Cirrus Logic Motorola Rockwell Telecommunications Texas Instruments
<b>Middleware</b>	Aurora Systems Pronexus SoftTalk Symetrics Industries Teledata Solutions
<b>NetWare applications</b>	CallWave Technologies
<b>Telephony boards</b>	Analogic Ariel ConnectWare Dialogic Rhetorex



## COMPUTER TELEPHONY

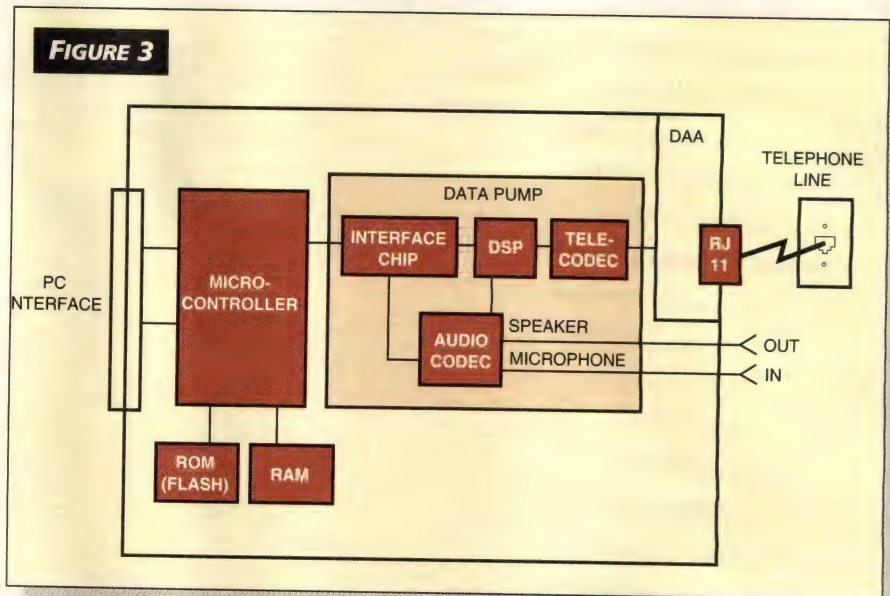
audio codec. This codec can be part of the modem or part of a multimedia audio system, such as a sound card. If the codec is part of the modem, the user can employ a headset or an analog telephone handset for the voice port. If the codec is part of a multimedia audio system, the user can have a speaker phone. Both the codec and modem can also be part of the sound card, as with IBM's Mwave product family.

### Software becomes vital to CT

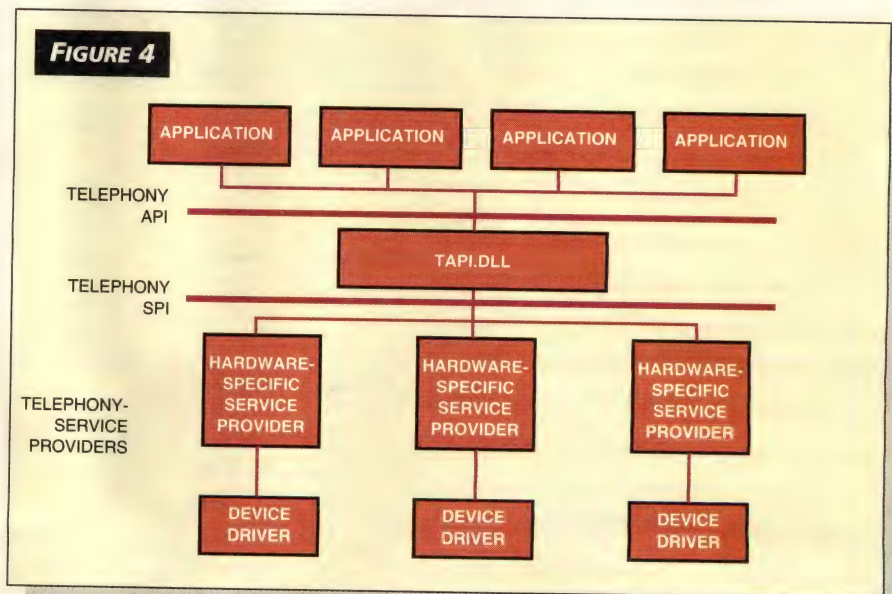
With all the processors involved in a telephony modem, software becomes a vital part of computer telephony. Each of the computer telephone's processing blocks has its own software needs. The controller and data pump, for instance, need programs for modem emulation, DTMF coding and decoding, line echo canceling, acoustic echo canceling (for full-duplex speaker phone), error correction, formatting, and call-progress control. The system may also include advanced features, such as text-to-speech conversion and voice recognition.

Many of these software blocks are available in libraries. Some libraries come directly from the DSP chip manufacturer. EDN's annual DSP Chip Directory (Ref 1) lists DSP chips and their support software. You can also obtain software from DSP development-tool vendors, such as Spectron and Spectrum Signal Processing, and from independent software vendors, such as VoCal Technology and Delrina. The speed with which the CT market is growing has stimulated the emergence of yet another software source, independent algorithm developers. These companies, such as HotHaus, provide application-specific software rather than libraries of generic telephony functions.

In addition, the host system has its own software needs, many of which relate to handling call-control functions, such as dialing and answering-machine emulation. In this host software, the TAPI block serves as a common interface between applications and the hardware-specific drivers (Fig 4). On the hardware side, TAPI, free



Several hardware blocks connect the PC to the telephone network. Designers have multiple choices for implementing each block, however, so the design is not as simple as it looks.



TAPI software sits between the application and the hardware layer, isolating the two. This isolation simplifies application design by eliminating the need to rewrite code for each telephone interface.

from Microsoft, provides a TSPI, which provides a link to hardware-vendor-supplied drivers. TAPI versions for Windows 3.1 are available over the Internet (Table 2). TAPI will also be an integral part of the Windows 95 operating system.

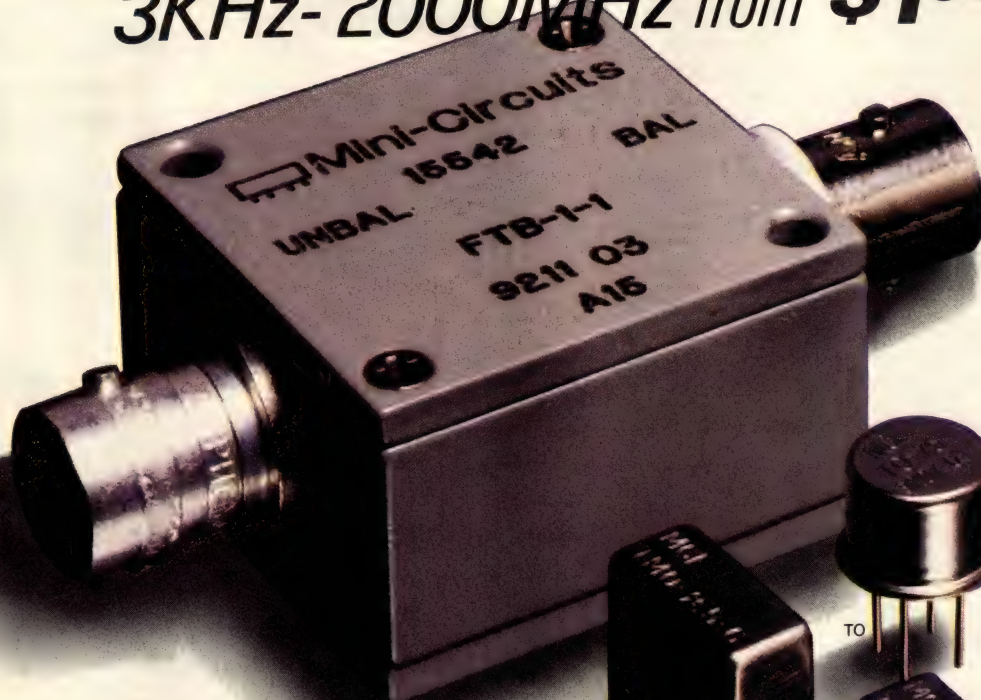
Although TAPI provides a path for controlling telephony functions, it does not provide a link to the audio data itself. Other application-program interfaces (APIs) under the Windows Open Services Architecture must fill that need. For instance, if the audio



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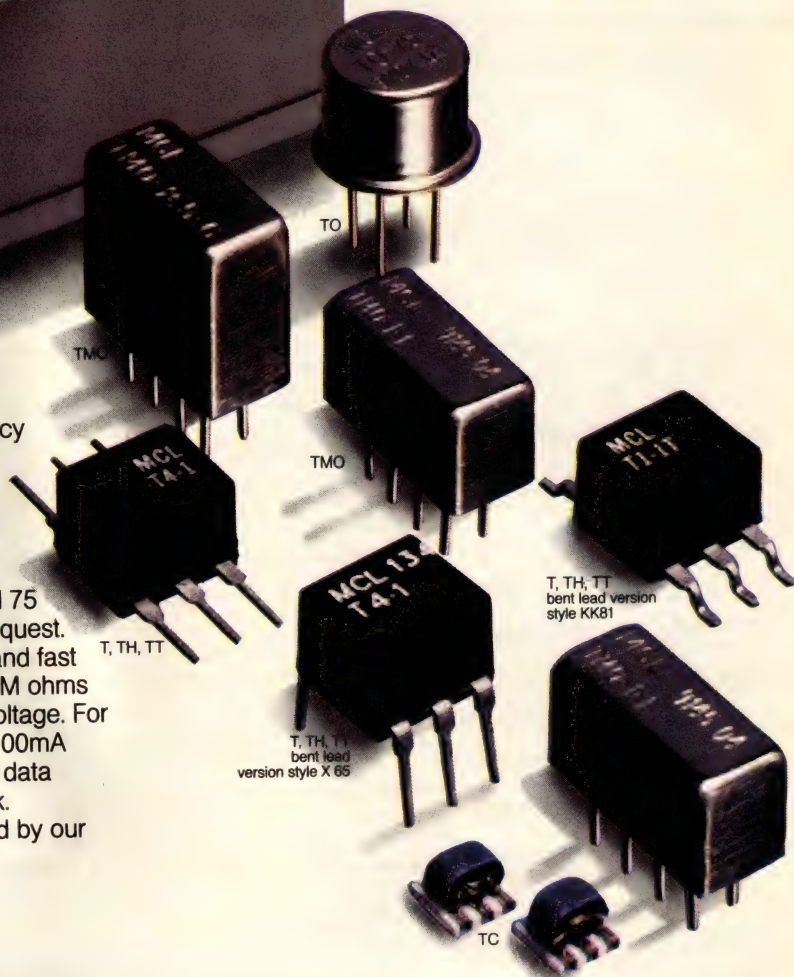
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## COMPUTER TELEPHONY

data is to pass through a sound card, the Wave API for handling audio files serves as the link to telephone audio. Many sources offer application software. Phoenix Technologies, for example, offers a Telephony Suite that provides speaker-phone, voice-mail, and fax capabilities. Radish Communications Systems offers a TalkShop program that lets your business call carry both data and voice.

Another class of software provider for telephony applications—the middleware provider—is also emerging. Middleware falls between end-user application and TAPIs, providing a means of rapidly producing custom application behavior without extensive programming. Aurora System's FastCall, for example, lets you specify behavioral rules so that you can customize the FastCall telephony func-

tions without writing a line of code. SoftTalk's Phonetastic and Symetrics Industries' Icon-O-Voice provide similar customizable applications.

**All the blocks are in place**

The wide and growing availability of telephony software and hardware shows that all the blocks are available to build telephony functions into your system designs. Table 2 gives a repre-

## MANUFACTURERS OF COMPUTER-TELEPHONY PRODUCTS

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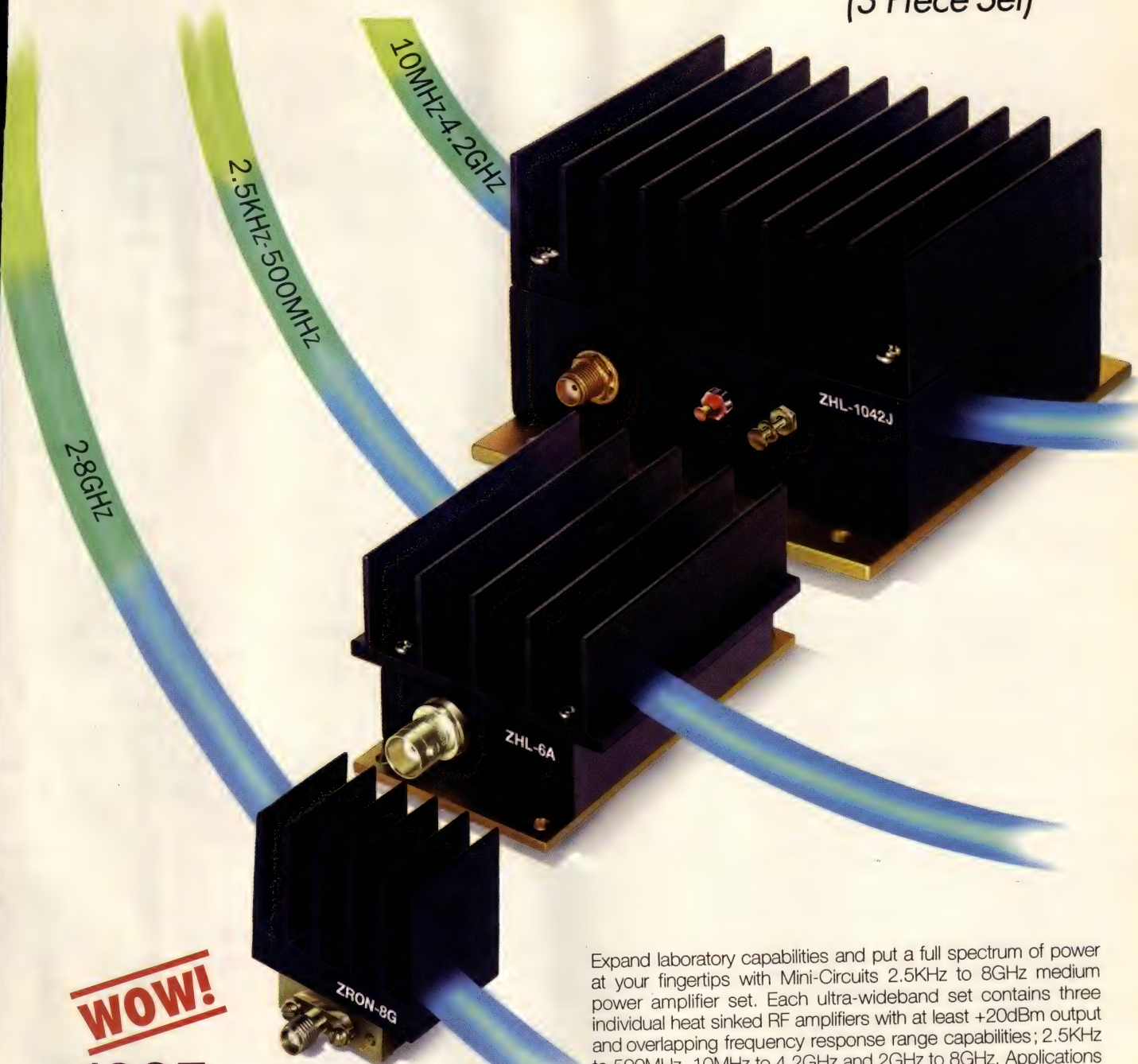
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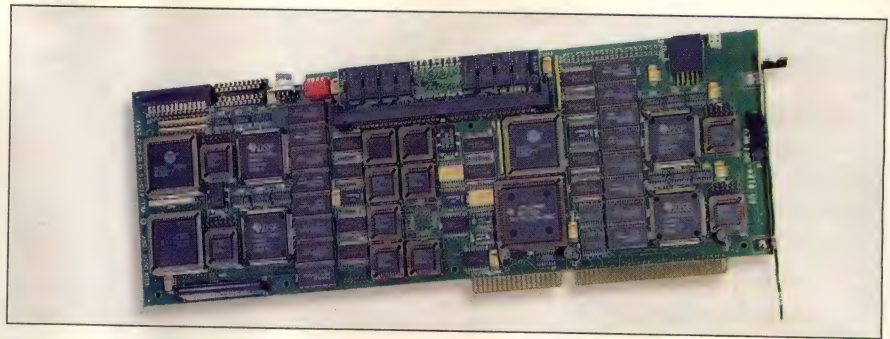


## COMPUTER TELEPHONY

sentative sample of vendors for the various blocks. However, carefully consider how those blocks fit together, and look carefully at the network to which the system must connect. Although applications programs hardly care, the hardware interfaces to various network types differ widely. Know if your design connects to an analog PSTN, a digital PBX, the ISDN, or a cellular network. Also know which network provider you are using. PBX vendors are highly competitive and keep their system designs proprietary. Their competitive nature manifests itself, among other ways, in distinctive hardware interfaces and in unique call-handling methods and features. If you plan to connect your system's telephony features through a PBX, you must offer a hardware interface that matches the PBX's requirements. Less obvious is the fact that you may need to adapt application software to each PBX.

Glue software, such as TAPI and TSAPI, goes a long way toward isolating the application program from the network's specifics, but such software is not foolproof. Not all PBX systems have the same features. Make sure that the PBX offers the features your application needs, such as dialing, answering, and querying call status. TAPI defines a set of Basic Services that every system provides. Features such as call holding, transferring, and tone detection, however, are Supplementary Services, which the PBX may not provide.

Work is under way to correct this situation. The recently formed Enterprise Computer Telephony Forum (ECTF) is seeking to promote interoperability among software and hardware from different vendors. ECTF is working to



**Telephony boards, such as the Antares from Dialogic, bring PBX functions to the PC.**

achieve widespread agreement on CT implementations based on international standards.

The same variation that plagues PBX switches occurs in the public networks. In the United States, for example, features such as forwarding and conferencing are not uniformly available. Where they are available, the tones and codes for invoking them vary from region to region. In Europe, the situation is even more diverse. The operational characteristics of various nations telephone networks differ, as do their physical interfaces. Requirements for various European nations may conflict or even contradict each other (Ref 2).

### Emerging technologies

You also need to consider emerging telephony technologies for which several competing open standards exist. One such technology is the use of a single phone line for concurrent voice and data traffic. Three competing open standards exist for this voice-over-data technology. Radish Communications Systems and its licensees offer Voice-View, which multiplexes digitized and compressed voice with the data stream. AT&T offers an analog simultaneous

voice over data (ASVD) option. A group comprising Creative Labs, Hayes, Intel, Rockwell, and US Robotics has created a digital simultaneous voice over data (DSVD) standard that transmits digitized voice and data streams in different modulation bands. The three methods are incompatible. That incompatibility may not be a problem in a closed-end application, in which you control both ends of the telephone connection. The risk still exists that market forces may eradicate one or more of the competing methods, however.

Another set of competing standards arises in telephony-server design. The server that provides telephony access to the network may use several cards for multiple channels or to bring DSP boards to bear on voice recognition and text-to-speech synthesis. The ISA bus, however, isn't fast enough to handle the data, so telephony-card vendors created a data bus that connects boards via a ribbon cable. The two alternatives are the MVIP (multivendor-integration protocol), which Natural Microsystems created, and the SCSA (signal-computing-systems architecture), which Dialogic created and ECTF administers.

**TABLE 2—INTERNET SITES FOR COMPUTER-TELEPHONY INFORMATION**

Title	Description	Address
TAPI 1.0 Specification	Windows Telephony API	<a href="http://www.microsoft.com">http://www.microsoft.com</a>
TSAPI 2.0 Specification	Novell Telephony Services API	<a href="http://corp.novell.com/infohelp.htm">http://corp.novell.com/infohelp.htm</a>
TMAP	TAPI/TSAPI bridge	<a href="mailto:cathy.hancock.0188953@nt.com">cathy.hancock.0188953@nt.com</a>
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## COMPUTER TELEPHONY

Although each standard boasts many compatible products, designers face the risk that market forces will eventually eliminate one or the other.

There also remain areas of CT that have no guidelines at all. For example, what should happen when an attempt at conferencing or call forwarding reaches a busy signal is up to the application designer. Efforts to standardize these behaviors are only beginning.

A final complicating factor in the development of CT is that the computer and telephone industries have trouble communicating. The PC industry has focused on the desktop, open standards, and rapid technology evolution. The telephone industry has traditionally focused on large systems, proprietary designs, and long-term answers. The two industries thus speak different languages.

Despite all the rough edges, however, the elements for adding telephony functions to PC-based systems are available. The widespread installation of TAPI and TSAPI has removed critical economic barriers to applications development, resulting in an explosion of new software and hardware from which to choose. The field is changing rapidly, so you must track the status of standards. However, unbounded opportunity exists to merge two pow-

The evolution of computer telephony (CT) will occur rapidly over the next several years, with some of the more profound changes affecting standardization. The telephone industry has been riddled with closed, proprietary designs and conflicting national standards. All that is changing.

The TAPI (telephony application-programming interface) and TSAPI (telephony services application-programming interface) were the first steps in making telephony networks more accessible to designers. Other steps include a move in Europe to adopt the

erful information-handling tools into one that is greater than the sum of its parts.

EDN

## References

1. Levy, Markus, and James Leonard, "1995 DSP Chip Directory," *EDN*, May 11, 1995, pg 40.
2. Dwyer, Joseph M, "Design your way through the maze of European telephone-company equipment," *EDN*, June 8, 1995, pg 147.

## LOOKING AHEAD

Net4 public-switched-telephone-network interface standard to consolidate the requirements of several countries. Another effort just beginning is the formation of Versit, a joint effort by Apple, AT&T, IBM, and Siemens to provide for applications that existing standards don't cover.

The result of all this standardization activity will be a host of innovative CT applications coming to a unified market that may have been uneconomical while telephony was a highly proprietary business.



You can reach Technical Editor Richard A. Quinnell at (408) 685-8028; fax (408) 685-8028\*.

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## COMPUTER TELEPHONY'S MANY EXTENSIONS

Ask a group of people to define "computer telephony" (CT), and you will probably get more answers than the number of people you asked. To some, the term implies coordinated operation between telephones and computers. In their vision, a phone rings at a sales office, and the computer network uses caller identification from the incoming call to switch the call to an appropriate salesperson. At the same time, the network sends the caller's database files to the salesperson's desktop computer. The caller's file pops up on the answerer's computer before the phone rings twice.

To others, CT implies using PCs to control telephones. These people envision CT users working with graphical interfaces rather than memorizing arcane numeric codes to invoke telephone features. Call forwarding and conference calls become mouse clicks instead of a tap dance on the telephone keypad.

Still others see PCs replacing private-branch exchanges (PBXs) as the telephone switches in small offices. These PC-based telephone systems not only can pass calls to office workers, but also can provide intelligent answers of their own. Voice-recognition software allows automated handling of information requests and order entry.

With enough processing power, CT can even become an electronic answering service. Voice recognition gives users of remote phones verbal control over telephony functions. Character recognition and text-to-speech conversion then allow these remote users to retrieve telephone, fax, and electronic-mail messages as audio in a unified messaging system.

The common element in these many visions is an extension of the user's ability to handle information. By combining the PC's versatility with the telephone's connectivity, CT provides a capability that is only beginning to be tapped.



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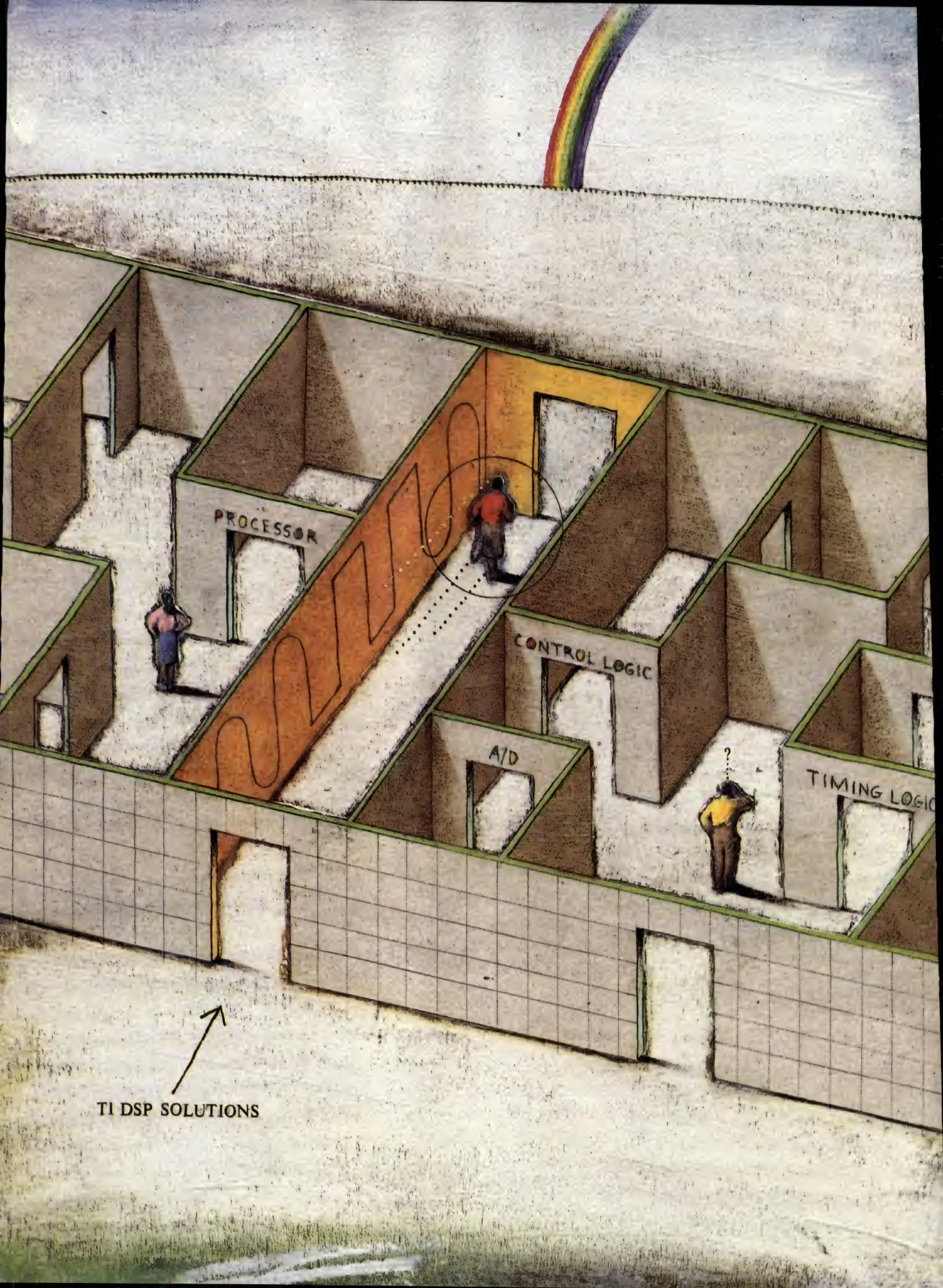
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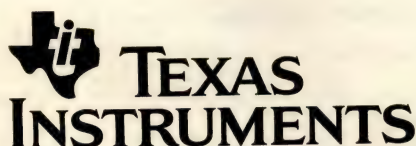
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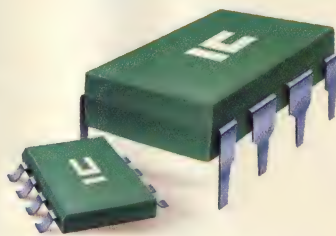


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# CONVERTERS

## *restructure communication architectures*

**BILL SCHWEBER, TECHNICAL EDITOR**

Until recently, improvements in A/D (or data) converters' speed, accuracy, and resolution have had minimal impact on communications systems. Of course, converters are used extensively to digitize baseband information-bearing signals, which is a signal-format issue, not a fundamental architectural change. The classic Armstrong superhet design—with a local oscillator and mixer feeding an intermediate-frequency (IF) stage—so neatly separated and solved RF-tuning, selectivity, sensitivity, and demodulation problems that it's difficult to see where improvements can be made, except by integrating more of the functional blocks onto a single device.

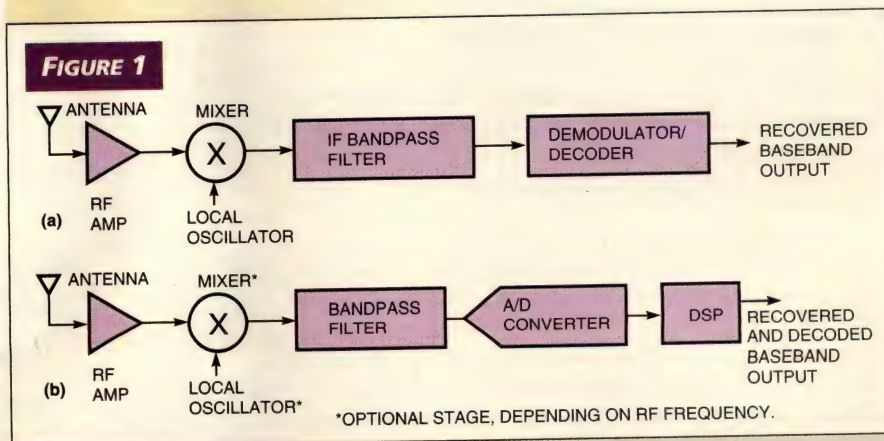
All this is changing. Wide-bandwidth converters, coupled with appropriately characterized dynamic performance, enable a new converter architecture that moves the digital circuitry closer to the receiver front end and antenna. This technique (known as digital IF, bandpass sampling, IF sampling, or digital-to-baseband conversion) means that a much greater percentage of the receiver circuitry is implemented by purely digital circuitry. This, in turn, allows more of the receiver functional blocks to be put on fewer VLSI ICs, thus moving communications design toward a "three-chip" solution: an analog front end optimized for interfacing to the antenna or channel; an IF-to-baseband A/D converter, associated digital circuits, and DACs; and a software-driven processor that extracts and demodulates the desired signals, which can be either digital or analog.

**The superheterodyne-receiver structure has served designers well for more than 70 years. Now, its reign is being challenged by A/D converters, which push digital circuitry closer to the antenna. As a result, you must understand a different set of converter specifications, as well as the hardware trade-offs of a software-based solution.**

At the same time, there are distinct limitations on what you can achieve with this architecture and what the cost in circuitry and software will be. The approach assumes that you know many of the parameters of the received baseband signal (fortunately, this is often the situation). If implemented improperly, your receiver can suffer from more than just "slight mistuning" and can produce useless strings of recovered signals and data.

### **Forget the old rules**

A receiver's life isn't easy: It performs three major functions while encountering hostile real-



In (a), a basic superhet receiver takes an amplified RF signal, mixes down to an IF using a local oscillator, then demodulates (decodes) the fixed-frequency IF signal. A double-conversion receiver includes another mixer/LO/IF stage after the RF amp. In digital IF down-conversion (b), the RF (or IF signal, depending on carrier frequency) is bandpass-filtered and then undersampled; the resultant sample values are processed within the DSP to produce the recovered signal.



## COMMUNICATION CONVERTERS

world challenges. First, the receiver must tune (select) the desired carrier frequency (channel) and then amplify the weak tuned signal. Finally, it demodulates the tuned and amplified signal so that you can recover the baseband information. The receiver performs these functions despite received

signal strengths at the antenna spanning and randomly varying over 100 dB of dynamic range (with typical signal values from -120 to -10 dBm), under difficult S/N-ratio conditions (0 to 50 dB), and with large adjacent signals making circuit linearity critical so that weak signals will not be obscured.

By mixing a broadband front-end signal with a local-oscillator (LO) signal, a traditional superhet design (Fig 1a) solves the problem of selecting a single carrier signal from within the broader spectrum. The LO is offset from the desired carrier by a fixed amount, such as 455 kHz or 10.7 MHz. The mixer pro-

### NYQUIST, UNDERSAMPLING, AND OVERSAMPLING

Many engineers remember two simple rules about Nyquist's 1929 sampling theory: You have to sample at a frequency that's *at least* twice the signal bandwidth (in practice, it's usually at least 2.5 times the bandwidth to provide some margin). And not doing so—called "undersampling"—leads to aliases, which are *always* bad. (A corollary of this theory is that you must put the signal to be sampled through a good lowpass filter to eliminate signals outside the Nyquist bandwidth.) So, how does always-to-be-avoided undersampling result in a viable receiver architecture?

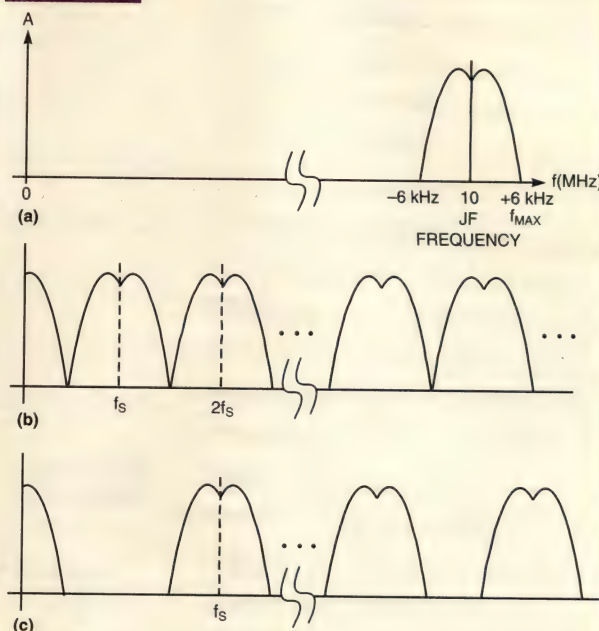
It's not that Nyquist was wrong but, rather, what we remember (or were taught) is a simplification. Nyquist's theory stipulates that you must sample at a rate of twice the *bandwidth of interest*. If you have a 6-kHz voice signal that is amplitude-modulated onto a 10-MHz carrier, the bandwidth of interest is just  $\pm 6$  kHz = 12 kHz, not  $10 \text{ MHz} + 6 \text{ kHz} = 10.006 \text{ MHz}$  (part **a** in Fig A). By undersampling this modulated signal at  $>24$  k samples/sec, the spectrum of the signal is "folded back" to baseband (part **b**). The alias contains the sample values that represent the original modulating signal spectrum, but now these values are at baseband instead of at the carrier (or IF) frequency. Undersampling, also known as "IF" or "bandpass" sampling, has shifted the signal spectrum as well as digitized it, functioning in one action like the LO, mixer, and IF bandpass filter of the superhet design.

When undersampling, the filtering requirement differs from sampling at the Nyquist rate of twice the highest frequency present. Instead of a lowpass filter extending just beyond the sampled signal spectrum, you now need to precede sampling with a bandpass filter centered around the modulated signal spectrum.

Potentially confusing the issue is oversampling. For all the virtues of undersampling, you have to worry about adjacent signal energy just outside the spectrum of interest. It's difficult (or expensive) to build a bandpass filter that is flat in the passband and has high attenuation outside the passband. In reality, the cutoff is more gradual, and some signal spectrum "leaks" through, overlapping with the spectrum of other aliases. The result is corrupted sample data, which cannot be recovered, and loss of available dynamic range. Your solution is to sample at multiples of the minimum value indicated by the Nyquist criteria. This move avoids overlap by spreading the aliased spectra of the sampled values apart; it also eases the filtering requirements (part **c**).

Another benefit of oversampling is that it increases SNR by 3 dB every time the sampling rate doubles. This process gain doesn't occur because total noise energy decreases. Instead, it results from the sampling action spreading the total noise energy over an increasingly wide spectrum, with a greater proportion of the noise placed outside the signal spectrum.

FIGURE A



$$\frac{(2x f_{IF}) - BW}{k} \geq \frac{(2x f_{IF}) - BW}{k+1}$$

WHERE  $k$  = ANY POSITIVE INTEGER,  
 BW = INFORMATION BANDWIDTH,  
 $f_{IF}$  = INTERMEDIATE FREQUENCY,  
 $f_s$  = SAMPLING FREQUENCY  $> 2 \times BW$ .

A 10-MHz carrier amplitude modulated by a 6-kHz signal has a bandwidth of  $>10$  MHz (a), but the actual information bandwidth is 12 kHz. By undersampling at exactly the Nyquist frequency (b), the information signal is "folded" into a series of aliases beginning at the baseband. Oversampling beyond the minimum Nyquist frequency spreads the aliases apart (c), reducing the cutoff demands on circuit filters.



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duces sum and difference frequencies; the sum frequency is filtered out in the IF stage; and the fixed-frequency difference signal is further amplified, filtered, and passed to a baseband stage for demodulation (decoding).

Nothing in the superhet design restricts the type of modulation used (AM, FM, or PM) or the signal type (analog or digital) as long as you choose appropriate values for front-end, IF, and demodulation-stage parameters. One of the major virtues of the Armstrong superhet is that it allows you to set these circuit parameters independently of each other, with minimal interaction and, thus, to optimize each for the bandwidth, noise, modulation, and signal type at each stage.

Digital IF stages are not just implementations of the classic superhet using as much digital circuitry as possible (such as a digital LO). Instead, the digital IF stage uses a completely different approach to the problem (Fig 1b). Its core consists of an A/D converter that takes the RF or IF signal and deliberately undersamples it, thus bringing the information-bearing sidebands of the carrier down to baseband frequencies. (As in a double-conversion super-

het, you first may have to down-convert the RF signal to a lower frequency when the carrier or first IF is too high for today's converters.) Computational circuits—usually a DSP—then extensively process this undersampled signal to extract the original baseband information. Although undersampling may seem to violate fundamental rules about Nyquist-rate sampling, it doesn't (see box, "Nyquist, undersampling, and oversampling").

Potential performance-related advantages of digitally based receiver architectures parallel the virtues of digital circuitry in other signal-processing and signal-control applications. Your need to "tweak" circuitry to compensate for temperature drift and component tolerances is greatly reduced. You can use the same circuitry for different signals (bandwidths, modulation, encoding, channel spacing) because so much of the functionality is software-configurable. In an extreme case, you can employ a single converter and DSP to serve many signals at the same time—within the whole band of interest (see box, "The software radio: one converter for all").

You judge an A/D converter used for IF-

to-baseband conversion using specifications that often differ from those used for converters intended for data acquisition. The repetitive characteristic of the input is one factor. Another important factor is that the bandwidth of the input signal to be digitized may be many times greater than the sampling rate—a situation that doesn't occur in conventional data-acquisition roles.

Begin your converter analysis with the traditional differential nonlinearity (DNL) and integral nonlinearity (INL) measures. DNL indicates variations of code width from the ideal 1-LSB value; increases in DNL, which generally occur with higher input frequencies, appear as an increase in quantization noise and a rise in the converter's noise floor. (Theoretically, rms quantization noise for an ideal converter equals the value of a LSB divided by  $\sqrt{12}$ .)

INL measures center deviations of each converter code from the ideal, straight-line transfer function (as drawn through the transfer-function endpoints or as a best-fit straight line through the data points). Such deviations, or bends in the straight-line transfer function, result in the converter's generating harmonics and spurious

### THE SOFTWARE RADIO: ONE CONVERTER FOR ALL

The digital approach also offers system designers another strategy for efficiently handling different signals simultaneously in a broadband. For example, a cellular base station may have to support analog cellular service as well as various formats and protocols of digital cellular service. Whether using conventional superhet designs or digital baseband conversion, the base-station designer must decide on a suitable mix of front-end interfaces—so many for the analog signals, so many for this digital standard, and so many for this other digital standard. A multistandard base station not only becomes costly in terms of hardware and power, but also makes it hard for you to get the mix of physical interfaces just right. Inevitably, as channel traffic patterns fluctuate, you'll have some interfaces that are underused while others are oversubscribed, causing callers to wait.

However, by using a "software radio" technique (Ref 2), you can avoid the problem of optimizing the needed interface mix. In a software radio, the A/D converter digitizes the entire band—with all its embedded channels. The DSP then applies the appropriate signal-processing algorithms to the aggregate samples, dynamically allocating channel-format assignments. The mix of signal types (and interfaces) is a func-

tion of software, so the hardware is used to its maximum.

Note that a software radio's wideband sampling is fundamentally different from down-converting a single wideband signal. In the former case, the wide bandwidth results from the large number of independent signals being converting simultaneously; in the latter case, the system is digitizing just one signal. In fact, a software radio could be operating on a bandwidth that is actually less than a single-channel system.

The software radio has some aggressive specifications. Of course, the DSP must be relatively powerful to run multiple copies of the different algorithms simultaneously to "tune" and "decode" all the input signals. Yet, the real burden falls on the A/D converter, which must have outstanding linearity to keep intermodulation distortion (IMD) low enough among the many input signals with their widely varying signal strength, so that false intermodulation products do not swamp actual signals. Vendors of converters for software-radio applications test them for IMD using more than just two or three tones simultaneously. For example, the Analog Devices AD9042 is tested with up to eight tones, and that number will be increased to 48 simultaneous tones to confirm the device's suitability for base-station software radios.



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frequencies that were not present in the original waveform being digitized.

The type and magnitude of these new signal components are better described by frequency-domain specifications (Fig 2), including an alphabet soup of SINAD (signal-to-noise and distortion), S/N ratio, SFDR (spurious-free dynamic range), and ENOB (effective number of bits), along with the more familiar THD (total harmonic distortion) and IMD (intermodulation distortion). Vendors test their converters by feeding a pure tone (or tones) to the converter and analyzing the resulting stream of data with FFT and other analyses. Both the input frequency and the sampling rate should be specified, of course.

SNR is classically based on the ratio of the rms signal value to the rms noise value, where the noise does not include the fundamental frequency or the first five harmonics:

$$\text{SNR (dB)} = 20 \log \left[ \frac{V_{\text{SIGNAL (rms)}}}{V_{\text{NOISE (rms)}}} \right]$$

Because the S/N ratio doesn't include the major harmonics, it is not truly indicative of the converter's dynamic range. For that measure, you'll need to use SINAD and ENOB. What SNR does tell you, however, is how close the actual noise floor is to the theoretical value.

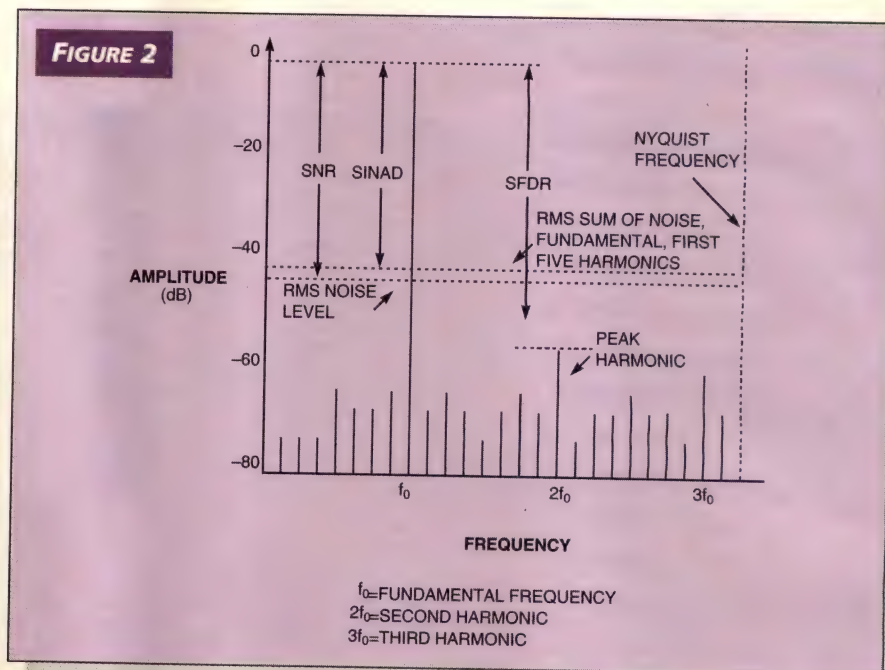
SINAD uses the same formula as S/N ratio but replaces the rms noise-voltage value with a voltage that includes all spectral components below the Nyquist frequency, except for fundamental and dc. Typical SINAD values for converters range from 40 to 60 dB, usually a few decibels less than the corresponding S/N ratio.

### ENOB, SFDR are critical

Using SINAD, you can calculate an overall indication of the converter's accuracy and dynamic performance, or ENOB, using

$$\text{ENOB} = \frac{\text{SINAD (dB)} - 1.76}{6.02} + 20 \log \left( \frac{\text{FULL-SCALE AMPLITUDE}}{\text{ACTUAL INPUT AMPLITUDE}} \right)$$

The closer the ENOB is to the converter's nominal resolution, the better the



**Key merit figures are determined by amplitudes of the fundamental, spurious signals, and noise levels, measured over various bandwidths.**

device's dynamic performance. ENOB values are typically 1 to 2 bits below nominal resolution. ENOB decreases with increasing frequency, so make sure the frequency you'll be using is covered by the vendor's specification. Some applications require ENOB specs of 10 to 11 bits; others need only 6 to 7 bits.

Note that this formula comprises two terms. The second term recognizes that ENOB will increase if the applied signal amplitude is less than the converter's full-scale span. Although it is a relatively small factor compared with the first term (unless the applied signal is much smaller than full scale), check to see if the SINAD conditions are comparable when looking at converters from different vendors.

Another indication of the converter's nonlinearity is its SFDR. SFDR is the ratio in dBc (decibels with respect to the carrier value) of the fundamental's rms amplitude to the next largest spur (spectral component) when the input is a single tone. Although this spur is often related to a harmonic of the fundamental, it doesn't have to be. For example, the converter clock, which is not directly related to the input signal frequency, may be coupling in to the

converter due to the circuit layout and crosstalk. SFDR values range from 50 to 80 dB, typically, depending on specific converter and test conditions.

Along with SFDR, THD quantifies the converter's nonlinearity using the ratio (in dBc) of the rms noise amplitude to the rms signal (single-tone) amplitude, where the noise is measured by summing the first few harmonic components. Most tests sum through the first five components for completeness, because the second and third harmonics contain most of the distortion power.

### Multiple signals, multiple tones

A communication system normally must deal with a signal spectrum that contains more than just a single component at a time (which, after all, would convey little information). This puts a premium on device linearity. The converter's IMD is tested with two nonharmonically related tones of approximately equal amplitude. When there is any nonlinearity in the signal path, these tones (at frequencies  $f_1$  and  $f_2$ ) generate harmonic-distortion terms at integer multiples of  $f_1$  and  $f_2$ , plus intermodulation (IM) tones at  $mf_1 + nf_2$ .



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(where  $n$  and  $m$  are any integers).

IMD is calculated using the ratio of the rms sum of the first IM terms to the rms value of the sum of the two applied tones. One issue to consider is the number of IM terms to be included. Most vendors include through the fifth order, where the order is defined as  $|n|+|m|$ , since second- and third-order terms usually dominate. Available IMD specs range from  $-70$  to  $-90$  dB.

You probably will be most concerned with the third-order term, due to the "near-far" problem. When two relatively strong adjacent signals occur at  $f_1$  and  $f_2$ , they can produce third-order terms at  $2f_1-f_2$  and  $f_1-2f_2$ , which fall close to either  $f_1$  or  $f_2$ , thus masking a relatively weak in-band adjacent signal. To better replicate real-world conditions, some vendors are also quantifying IMD performance with more than two simultaneous tones.

Sampling-time-aperture issues are also critical. Ironically, aperture delay—the lag between the ideal "requested" sampling instant and the actual sampling time—may be an important data-acquisition parameter, but it is not a factor in communications

applications because the sampling action is repetitive. What does matter is aperture jitter, the uncertainty and variation in sampling time caused by internal converter noise and clock jitter. This jitter noise phase-modulates the sampling time, limiting the maximum  $dV/dt$  input slew rate—and,

hence, maximum frequency—that will have a  $dV$  error less than  $1/2$  LSB:

$$\text{MAXIMUM INPUT FREQUENCY} = \frac{1}{t_A \cdot 2\pi \cdot 2^{n+1}}$$

where  $t_A$  is rms aperture jitter and  $n$  is the nominal converter resolution. The effect of timing jitter on SNR is

## LOOKING AHEAD

You'll see increased use of digital-to-baseband techniques, in both high-volume, highly standardized cellular-phone applications, as well as in base stations where signal flexibility is a real benefit. In addition, more converter and S/H vendors are optimizing their designs and specifying them for undersampling applications, at rates and bandwidths matched with various communication standards and traditions, such as sampling for US analog-cellular phones at  $>1024 \times 30$ -kHz channel bandwidth=30.72M samples/sec, for example. They'll include low-speed D/A converters for controlling the still very necessary front-end AGC and related functions, plus D/A converters for signal synthesis.

IC and system designers will add wideband Gaussian noise to the signal input (dithering) to better randomize quantization noise and increase dynamic range by 10 to 20 dB. Vendors are exploring how sigma-delta A/D architectures can be adapted to undersampling, specifically by changing the conventional lowpass digital filter of the converter modulator to a bandpass filter. Finally, more dedicated digital preprocessors (such as the Harris HSP50016) will be developed. These ICs take a high-rate A/D output data stream and perform several stages of decimation and filtering, producing an output data stream that requires less processing by the DSP.

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$$\text{SNR}_{\text{JITTER}} = 20 \log \left( \frac{1}{2\pi f t_{AJ}} \right)$$

Timing jitter reduces the effective S/N ratio you can achieve, raising the noise floor that the basic S/N ratio equation indicates:

$$\text{SNR}_{\text{TOTAL}} = -10 \log \left[ 10^{\left( \frac{-\text{SNR}_{\text{JITTER}}}{10} \right)} + 10^{\left( \frac{-\text{SNR}_{\text{JITTER}}}{10} \right)} \right]$$

Note that this specification assumes you are providing a jitter-free conversion clock to the converter or its S/H circuit. Your clock-source quality and careful signal routing (to minimize noise and crosstalk) are critical. For example, just 20 psec of rms jitter on a 12-bit converter with a 1-MHz input reduces S/N ratio by 1.5 dB. If your analysis shows that applied clock jitter may be a significant error factor, you should identify and reduce sources of jitter (see Ref 5).

Consider using an external S/H circuit to increase both SFDR and ENOB, even for converters that have an internal S/H. But be prepared to work out the two-chip error budget. Make sure the S/H you select offers low distortion in its hold mode at the frequency of your input signal. Note that many S/Hs are specified for distortion when tracking, and the corresponding hold-mode figures may be harder to find.

Driving the A/D converter properly is critical (see Ref 6). Most sources have a 50 $\Omega$  impedance; any mismatch or distortion in your signal path will degrade achievable performance. Even if all the converter specs are sufficient, you still have to examine the device and circuit bandwidth. Full-power bandwidth is the critical parameter for your digital-IF-to-baseband technique to work properly. Although

there are many definitions of bandwidth, the most common uses the traditional -3-dB point, where the converter's reconstructed input is 3 dB below its low-frequency value.

Normally, you don't want to operate near this 3-dB point, however. By operating the converter in the relatively flat zone (well below the 3-dB point), you'll minimize inadvertent gain-and-phase distortion. Also, consider the limitations of any input buffers or layout between your analog input signal and the converter's input.

Be sure that the vendor specifies input bandwidth using a full-scale signal (several volts) rather than a small-signal input (10s of millivolts). Small-signal inputs can yield especially favorable results; they don't stress the converter fully, because they don't cause slew-rate limitations or other

**TABLE 1—REPRESENTATIVE A/D CONVERTERS FOR COMMUNICATIONS**

Vendor	Device	Bits	Sample rate (Msamples/sec)	Bandwidth (MHz)	Power	SNR* (dB)	SINAD (dB)	SFDR (dBc)	THD (dBc)	IMD (dBc)	Price
Analog Devices Circle No. 301	AD9042	12	41		5V/575 mW	70		-80		-90	\$200 (1000)
	AD876	10	20	150	5V/160 mW		51	-65	-60		\$10 (1000)
Analogic Corp Circle No. 302	ADC3120	14	20	80	$\pm 15$ , +5, -5.2V/4W	75		-90	-82		\$3500 (10)
Burr-Brown Corp Circle No. 304	ADS7819	12	0.8	1.5	$\pm 5$ V/225 mW	70	70	-77	-82		\$22.15 (100)
	ADS605	12	10		$\pm 5$ V, 220 mW	66	63	-63	-70		\$125 (100)
Comlinear Corp Circle No. 305	CLC949	12	30	100	5V/400 mW	65		-72		-70	\$98 (1000)
Datel Inc Circle No. 306	ADS-946	14	8	10	$\pm 5$ V/1.9W	74	70		-73	-82	\$381 (100)
	ADS-945	14	10	50	$\pm 15$ , +5, -5.2V/4.2W	78	74		-80	-84	\$866 (100)
Harris Semi- conductor Corp Circle No. 307	HI1386	8	75	150	-5.2V/580 mW		41				\$48 (1000)
	HI5702	10	40	250	5V/390 mW	57	56	-63	-60	-59	\$35 (1000)
Linear Technology Corp Circle No. 308	LTC1410	12	1.25	20	+5V/160 mW		68		-82	-84	\$23 (1000)
Maxim Integrated Products Circle No. 309	MAX153	8	1	1	5V/40 mW		45	-50	-50		\$6.63 (1000)
	MAX100	8	500	1200	5, -5.2V/5.2W	45					\$265 (100)
Micro Linear Corp Circle No. 310	ML6401	8	20	80	5V/235 mW	44		-50	-46	-46	\$6.75 (1000)
National Semi- conductor Corp Circle No. 311	ADC12062	12	1		5V/75 mW	72	71		-82	-80	\$29 (1000)
	ADC12662	12	1.5		5V/200 mW	70	70		-80	-80	\$34 (1000)
Signal Processing Technologies Inc Circle No. 313	SPT7750	8	500	500	5V/5.5W	44	37	-41	-38		\$250 (100)
	SPT7840	10	10		5, -5.2/100 mW	57	56	-63	-59		\$9.60 (1000)
Sony Electronics Inc Circle No. 314	CXA1866Q	6	140	210	$\pm 5$ V/325 mW	32					\$20 (1000)

**Note:** Test conditions and definitions vary among vendors; check data sheets carefully.

\*SNR = S/N ratio.



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large-signal effects. Full-scale test inputs that are 0.5 dB below the converter's maximum input range are most commonly used.

### Specs and more specs

Dynamic specs are essential for determining a suitable A/D converter. There are some ways in which available component specs can be misleading. When the sampling frequency is coherent with respect to the input-signal frequency, the input-signal energy falls into one FFT bin. However, when the sampling isn't coherent—the ratio between signal and sampling frequencies is not the ratio of two integers—the waveform samples will smear into FFT bins around the fundamental.

To compensate, the vendor can establish a window around the fundamental bin. However, this option also reduces or eliminates noise energy that happens to be in these bins, thus affecting subsequent computations and improving some specs.

When you start evaluating potential converters (see **Table 1**), don't be surprised if some of the converters have video-application specs. Many communications converters were originally intended for video digitization, and many of the performance attributes and specifications are similar.

If you're deciding whether to pursue a digital-to-baseband approach, consider component cost, potential benefits, and complexity. The digital method is more than just a theory: It's

being used successfully in Global System for Mobile (GSM) cellular phones and its US equivalents, as well as in cellular base stations, which demodulate a variety of input formats such as US digital cellular, conventional Advanced Mobile Phone Service analog cellular, and others. These applications represent opposites in system flexibility: The phone unit is a single-format device, and the base station is a multiple-format system.

For either approach, you'll need an RF stage (and AGC) to capture the weak antenna signal, and you'll probably need a first conversion stage to bring the RF carrier down to a more manageable IF frequency. For getting the IF down to baseband, consider that a digital solution may be more expensive than an analog one, even with today's lower cost converters and DSPs. Existing analog techniques have been in place for so long that many low-cost and optimized mixers, gain-control blocks, IF filters, and demodulators are available.

Try to quantify the benefits and determine exactly what performance or implementation advantage each approach provides. Are you seeking improved bit-error rate (BER), audio fidelity, adaptability in performance, VLSI integration, or flexibility to handle different types of inputs? If you don't need the flexibility, for example, the digital solution may be solving a problem you don't have. Perhaps you can achieve your goals by circuit and com-

ponent optimization with a conventional superhhet.

Finally, consider the complexity and unknowns of your received signal and the signal uncertainties introduced by the medium you are using, whether it's air, copper cable, or optical fiber. Your received-signal-recovery challenge is divided into three categories of increasing difficulty (**Table 2** and **Ref 1**): signal detection (simply determining signal presence or absence), signal estimation (determining a signal value at one isolated time only), and continuous signal estimation (determining the value of a continuously varying analog signal). Any receiver design must be robust enough to handle the unexpected, such as noise bursts, carrier fading and dropout, multipath signals, and similar woes, by degrading as gracefully as possible rather than have sudden increases in BER or loss of analog performance.

For all three categories of signal difficulty, there is a hierarchy of challenge for the receiver. The challenge increases the less you know about the incoming signal. The simplest category is the relatively known signal-in-noise, which is followed by the signal-with-unknown-parameters-in-noise. Most difficult is the random-signal-in-noise.

As you move from the simplest case of signal detection for a known signal toward the most difficult case of continuous estimation of a random signal, the algorithms you need to embed in the DSP become more complex to

**TABLE 2—HIERARCHY OF SIGNAL-RECOVERY DIFFICULTY**

	Detection	Estimation	Continuous estimation
<b>Signals with known parameters</b>	Synchronous digital communication Pattern recognition	PulseAM, pulseFM, pulsePM communications systems with inaccuracies in inertial systems.	Conventional AM, FM, and PM with phase synchronization. Signal estimation in seismic/sonar systems. Synchronization in digital systems.
<b>Signals with unknown parameters</b>	Pulsed radar, sonar, target detection. Digital communications without phase reference. Digital communications over slowly fading channels.	Range, velocity, and angle measurements in radar and sonar. Discrete time analog communication systems (with unknown amplitude or phase variations in the channel).	Conventional AM, FM, and PM without phase synchronization. Estimation of channel characteristics when phase of input signal is unknown.
<b>Random signals</b>	Digital communications over scatter link. Passive sonar.  Seismic detection systems Radio astronomy (detection of noise sources).	Target parameter estimation in radar or sonar. Velocity measurement in radio astronomy. Power-spectrum parameter estimation.	Analog communication over randomly varying channels. Estimation of statistics in time-varying processes.





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develop and more time-consuming to execute. Implementing these algorithms efficiently is important because virtually all communication algorithms must execute in an isochronous mode, with the signal processed fast enough so that no incoming signals (or sample points) are missed.

Finally, consider where you will obtain the code to drive the DSP. If you have to develop the code yourself, it may be hard to determine how long it will take to implement, debug, and field-test your coded algorithms—and estimate the required memory, as well. Fortunately, for some standard communication applications such as GSM and digital cellular, DSP vendors and independent third parties offer code modules that are tested and benchmarked using specific vectors and patterns established by the standard. This, of course, greatly reduces the coding you have to do and the uncertainties you face.

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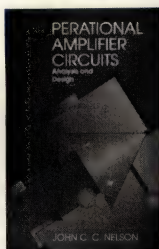
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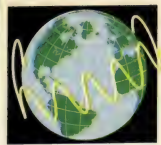
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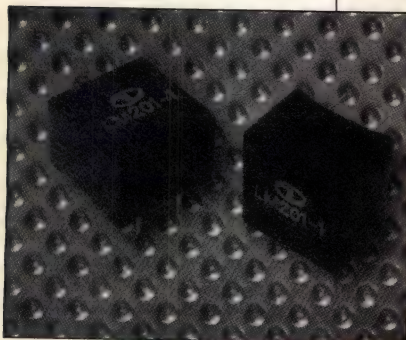


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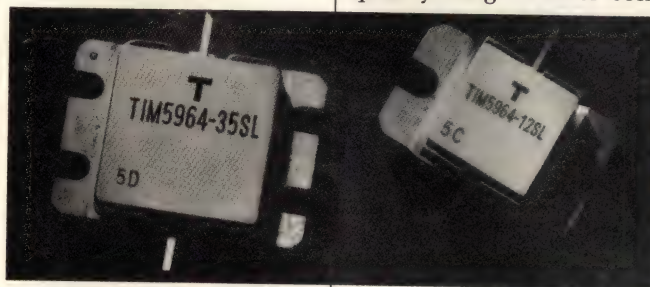
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## MIXER ICs FOR WIRELESS-COMMUNICATIONS SYSTEMS.

As a result of B6HF bipolar silicon technology, the PMB 2331, 2332, and 2333 ICs have a 0.4-μm structure size, low power requirements, and 2.5-GHz operating frequencies. Mixer-circuit PMB 2231 is a 2.7 to 4.5V, 1.6-mA Gilbert cell mixer that has highly isolated RF, local oscillator, and IF ports. Its noise figure is 8 dB. The PMB 2332 is a mixer and low-noise amplifier that has all the features of the 2331 as well as an integrated low-noise amplifier (LNA) with a gain of 10 dB and a noise figure of 3.3 dB at 2.5 GHz. The PMB 2333 mixer-and-driver amp circuit includes the fea-

tures of the 2331 and a driver amp with 10-dBm output power at 1-dB compression. \$1.23 to \$1.75 (10,000). **Siemens Components Inc.**, Cupertino, CA. (800) 777-4363 (request package M12P030).

**Circle No. 455**



## ▲ LINE OF GaAs FETs EXPANDS.

A 15W version of the 14- to 14.5-GHz internally matched Ku-band GaAs FET, named TIM1414-15, is geared toward applications such as very-small-aperture terminals. The device costs \$1550. In addition, the TIM5964-35SL, a 35W C-band GaAs FET, has lower power consumption, resulting in cooler operation and better system reliability. The series of C-band GaAs FETs targets applications such as mobile telecom ground stations, satellite uplinks and earth stations, radar, and digital radio links. Typical pricing for a 4W device is \$280; typical pricing for a 30W device is \$1350. **Toshiba America Electronic Components Inc.**, Irvine, CA. (800) 879-4963; (714) 455-2000.

**Circle No. 456**

## SURFACE-MOUNT IC FAMILY FOR WIRELESS APPLICATIONS.

This family of RF ICs suits wireless applications such as cordless phones and wireless LANs. The small-outline, surface-mount chips include three ICs for the transmit

path, two ICs for the receive path, and a PLL. The U2790B, for example, is a direct conversion I/Q modulator that operates from 100 to 1000 MHz; the U2791B is its companion direct conversion demodulator, which has a 100-MHz to 1-GHz frequency range. Power con-

sumption for the U2790B is 30 mA for output power of -1 dB and a sideband suppression of 40 dB at 900 MHz and 35 dB at 150 MHz; power consumption for the U2791B is 28 mA with a LO input level of -10 dBm, a double sideband noise figure of 12 dB at 950 MHz, and a third-order intercept point of 3 dBm. Prices for the ICs range from \$2.25 to \$5.75 (10,000). **TEMIC/Telefunken Semiconductors**, Santa Clara, CA. (800) 554-5565, ext 57.

**Circle No. 457**

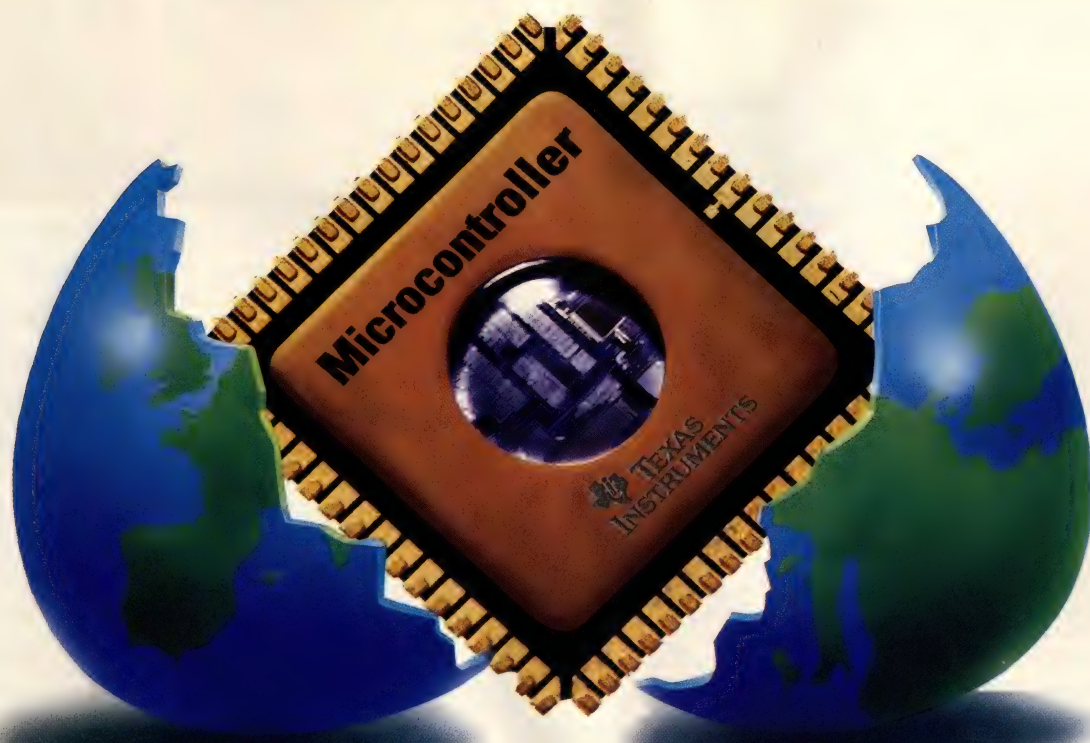
## LDMOS RF DEVICE FOR GLOBAL-SYSTEM MOBILE-COMMUNICATIONS APPLICATIONS.

The MHW913 laterally diffused MOSFET (LDMOS) power amplifier is designed for the European digital 8W global-system mobile-communications radio network. The power amp operates from a 12.5V power supply over a frequency range of 880 to 915 MHz; it requires <100 mW of RF input power. \$42.90 (low volumes). **Motorola Semiconductor Products Sector**, Phoenix, AZ. (602) 244-6900.

**Circle No. 458**



# We have good news...



## TI introduces a massive array of microcontrollers.

Finding exactly the right microcontroller for your design can often be a bewildering challenge. That's why TI has decided to make things simple. With the introduction of more than **20 new PRISM-based TMS370C8 and -C16** devices, TI offers an extended industry-wide line of integrated products. You can choose exactly the power, memory, peripherals, features, footprints you want without making compromises. From the entry level TMS7000 family through the field programmable TMS370 family and the new PRISM-based TMS370C8 and -C16 family, there's a TI microcontroller that's right for your application. And your budget. To make things even simpler, we have **a single development tool for each family** so you don't




have to learn new rules every time you change your design.

We even have a **low cost, entry level starter kit** so you can get a feel for how simple the TI development environment is. What's more, PRISM uses **reusable modules** so you can shave months off your design cycles and **gain valuable time to market**. And, you'll secure your

investments in development tools and engineering training for at least 10 years. Whether you're designing for **home automation, motor control, scales, electronic money, energy metering, alarms, etc.**, you name it, TI's microcontrollers can point you in the right direction.

To find out more, just circle the reader service number. It's as simple as that.

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 **TEXAS  
INSTRUMENTS**



## COPPER-BASED GBAUD LINK MODULE.

The copper-based GLM module complies with HP-IBM-SUN, Fibre Channel System Initiative (FCSI), Full Speed (1.0625-Gbit/sec), Gigabaud Link Module (GLM) specification. The VSC7115/VSC7116 Fibre Channel transmitter/receiver chip set forms the core of the VSC7181 GLM module but can be used separately from the module for other Fibre Channel applications. The module handles high-speed specifications and interfaces with Fibre Channel via a 20-bit 8B/10B encoded 53-MHz TTL bus, as defined in the Fibre Channel GLM specification. The VSC7181 GLM uses an industry-standard DB-9 style connector to transport Gbaud data up to 50m over high-bandwidth, differential cable assemblies. The VSC7181 is <\$200 (1000); the VSC7115/VSC7116 chip set costs \$70 (1000); the VSC7181EV evaluation kit, which includes two VSC7181s, one 5m cable, two loopback adapters, and documentation, costs \$995. **Vitesse Semiconductor**, Camarillo, CA. (805) 388-3700. **Circle No. 459**

## SURFACE-MOUNT HYBRID COUPLERS.

A family of six surface-mount, 90° hybrid couplers suits high-volume cellular and wireless applications. The couplers operate from 800 MHz to 2.7 GHz and measure 0.35×0.56 in. The units have 100W average CW power handling, 0.2-dB typ (0.3-dB max) insertion loss, and 25-dB typ (22-dB max) isolation. \$1.30 (OEM qty). **Anaren Microwave Inc.**, East Syracuse, NY. (800) 544-2414, ext 145. **Circle No. 460**



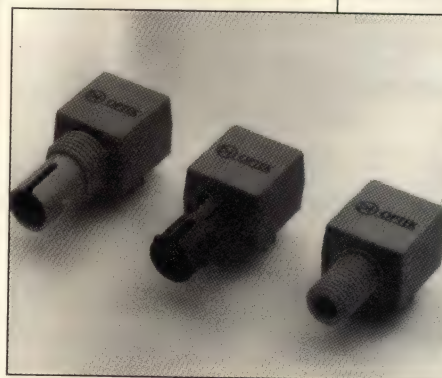
## LOW-COST HIGH-PERFORMANCE MIXER.

The ZP-860MH mixer is a miniature connectorized unit offering IF responses to dc. The mixer handles a frequency range of 800 to 1050 MHz. It has high L-R of 35 dB (typ) and L-I isolation (27 dB). Conversion loss specifications are controlled statistically to better than 4.5σ from mean. Absolute maximum ratings are 150-mW RF power and 40-mA IF current; operating temperature range is -55 to +100°C. \$47.95. **Mini-Circuits**, Brooklyn, NY. (718) 934-4500. **Circle No. 461**

## CORDLESS IR PCMCIA FAX MODEMS.

The Airplex cordless IR PCMCIA fax-modem series comprises the 2705, a V.32/V.32bis PCMCIA Type II fax modem, and the 2702, an IR jack/adaptor for use with PCMCIA fax modems. The series eliminates the need for any cord connections between a PCMCIA fax modem and the indoor RJ11 telephone jack, a result of the company's patented diffuse, omnidirectional infrared technology. The technology allows data transmission between Airplex PCMCIA fax modem or adaptor and a compact base transceiver (also included with the series), which interfaces to standard RJ11 analog phone jacks. The Airplex series provides interior mobility up to 1000 ft²; it supports 14.4-kbps modem

operation and, because of its diffuse IR technology, isn't dependent on line-of-sight transmissions. Airplex requires no special software or FCC licensing agreements. Model 2702 costs \$297; Model 2705 costs \$459. **K and M Electronics Inc.**, West Springfield, MA. (800) 597-4727; (413) 781-1350. **Circle No. 462**



## ▲155-MHZ FIBER-OPTIC RECEIVERS.

The OPF2408, OPF2418, and OPF2418T receivers suit use in ATM interfaces, computer networks, LANs, and modems. The devices couple a high-speed photodiode to a transimpedance amplifier. The OPF2418 suits use with an 850-nm, high-speed IR transmitter. The receivers are compatible with ST, SMA, and threaded-ST connectors. The OPF2418 costs \$27.94 (100). **Optek Technology Inc.**, Carrollton, TX. (214) 323-2200. **Circle No. 463**

## I/O HARDWARE FOR REMOTE ACCESS APPLICATIONS.

By supporting the Plug-and-Play capabilities of Windows 95, TurboPort/PnP I/O hardware takes the hassle out of installing new devices. Users simply click a mouse to install and configure I/O hardware, eliminating time-consuming DIP switches and jumpers. The serial I/O

controllers deliver fast, reliable connections for remote PC users by supporting data rates to 460.8 kbps, transcending the V.34 modem speeds and basic ISDN-to-PC transmissions. When inserted into an expansion slot of any ISA-based system, the half-card-format TurboPort controllers supply one or two high-speed serial ports

capable of handling ISDN terminal adapters and modem connections for Windows 95, Windows, Windows NT, Windows for Workgroups, OS/2, and Novell NetWare; the hardware accommodates 9600-bps, 14.4-kbps, and 28.8-kbps

(and above) modems. A one-port version costs \$109; a two-port version costs \$149. **Star Gate Technologies Inc.**, Solon, OH. (800) 782-7428; (216) 349-1860. **Circle No. 464**

## M-BLOCK MICROWAVE FILTER.

The M-Block Microwave Filter offers a 40% size reduction from previous surface-mount-device filters, suiting it for wireless-communication applications. M-Block has coplanar construction, which aids in component flatness on pc boards; it features true infrared reflow solderability; and, it has low RF leakage as a result of the filter's copper-plated outer surface. M-Block suits any portable wireless communication device that requires considerable miniaturization in the ISM and cellular frequency bands. A two-pole version costs \$1.50. **Murata Electronics North America**, Smyrna, GA. (404) 436-1300. **Circle No. 465**



# ...and we have more good news for microcontroller users

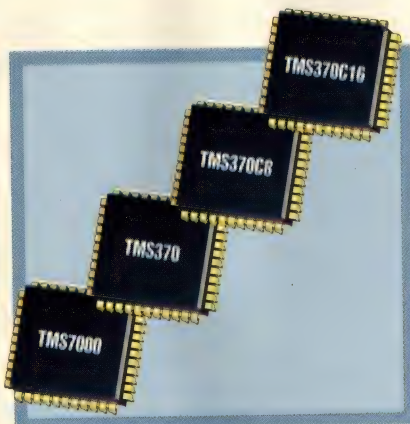


## TI delivers.

Finding the perfect microcontroller for your designs is one thing. Getting silicon delivered for your production is another. These days, microcontrollers can be found is virtually everything.

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To keep up with our commitment. From the entry level TMS7000 family through the field programmable TMS370 family and the new PRISM-based TMS370C8 and -C16 family, there's a TI microcontroller that's

right for your application. **And it's available in volume now.** Add to that a massive team of TI microcontroller experts, a Europe-wide network of distributors and a wealth of technical support documentation. In more ways than one, TI delivers. To find out more, use the reader service card. We deliver product information on time as well.

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**SIGNALING SOFTWARE  
FOR PROTOCOL AND  
TRANSMISSION TESTING.**

The user-to-network (UNI) signaling test software helps unravel the complexity of implementing switched networks. The software is designed for protocol and transmission testing of ATM and broadband-ISDN networks; it works in conjunction with the HP E4200/E4210 broadband series test system. UNI software accommodates a variety of standards, such as Signaling ATM Adaptation Layer (SAAL) ITU-T Q.2100, Q.2110, and Q.2130; Draft Q.SAALO; ATM Forum UNI Spec V3.0; and ATM Forum UNI Spec V3.1. HP also introduced the ATM and LAN protocol test application, the HP E4215A, which supports Internet protocol, ATM Address Resolution Protocol (ATMARP), and packets over ATM under RFC1577. HP E4214A B-ISDN UNI Signaling Test Software costs \$8400; HP E4215A B-ISDN LAN Protocol Test Software costs \$1030. **Hewlett-Packard Co.**, Direct Marketing Organization, Santa Clara, CA. (800) 452-4844, ext 9320.

**Circle No. 466**

**WIRELESS-LAN-  
DEVELOPMENT TOOL.**

The WaveRider tool comprises a pair of wireless-LAN nodes that let you evaluate the vendor's DE6003, a 2.4-GHz, frequency-hopping transceiver module. Each node includes the DE6003, a media-access-control (MAC) controller board, the WaveRider MAC protocol, and dual antennae. The nodes mount in a 2.5×5-in. plastic housing and interface to laptop and desktop computers via a parallel port. The system includes the Win-

dows-based Wireless LAN Diagnostics tool, which lets you modify packet lengths, monitor data throughput, examine packet details for error analysis, and perform an RF-site survey by monitoring RF activity on 83 channels simultaneously. WaveRider costs \$3250. **GEC Plessey Semiconductors**, Scotts Valley, CA. (408) 438-2900.

**Circle No. 467**



**OPTICAL POWER METER  
PROVIDES ON-SITE FIBER-  
OPTIC TESTING.**

The OLP-18 handheld optical power meter features a -60- to +26-dBm measurement range and operates across 800- to 1600-nm wavelengths. The device displays results on a four-digit LCD screen with 0.01-dB resolution; users can switch the screen to show watts or decibels referred to 1 mW. The meter has switchable wavelength settings of 850, 980, 1310, 1480, and 1550 nm. Using these wavelengths, an operator can simultaneously perform measurements at two wavelengths. With the company's OLS-15 handheld optical source or OLS-110 source module, the OLP-18 can determine the wavelength of alternating 1310- and 1550-nm signals. The device can also detect modulation frequencies of 270 and 330 Hz and 1 and 2 kHz. Price is

\$1730. **Wandel & Goltermann Inc.**, Morrisville, NC. (919) 460-3341.

**Circle No. 468**

**CLOCK-RECOVERY AND  
DATA-RETIMING IC.**

The MAX3270 clock-recovery and data-retiming IC suits 155- and 622-Mbps SDH/SONET and ATM applications. The IC meets Bellcore and CCITT jitter-tolerance specifications, ensuring error-free data recovery. The MAX3270 has differential ECL input and output interfaces, so it is less susceptible to noise in a high-frequency environment. The fully integrated PLL includes an integrated phase/frequency detector that eliminates the need for external references. The IC comes in 44-pin MQFPs screened for commercial 0 to 70°C temperatures. From \$39.50 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087.

**Circle No. 469**

**WIRELESS-LAN IC.**

The WL100 CMOS IC operates from a 5V supply and provides a standard 8-bit parallel interface to the vendor's 2.4-GHz, frequency-hopping DE6003 media-access-control (MAC) controller board. The devices provide all the physical-layer functions for a wireless LAN or other wireless-data applications. The interface allows the use of a variety of  $\mu$ Cs and  $\mu$ Ps to implement the MAC protocol function. It provides a variable-rate clock and data recovery, 32-bit cyclic-redundancy-check generation and validation, serial-to-parallel and parallel-to-serial data conversion, programmable preamble generation, automatic data-

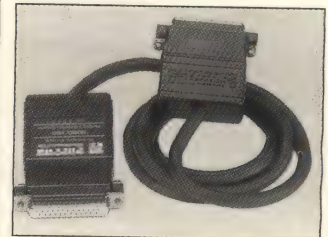
bit stuffing, automatic antenna-diversity selection, and battery-level monitoring. Price is \$10 (10,000). **GEC Plessey Semiconductors**, Scotts Valley, CA. (408) 438-2900.

**Circle No. 470**

**PUSH-ON LOCKING RF  
COAX CONNECTORS.**

The POD1 series push-on locking, RF coaxial connectors measure approximately one-half the diameter of most BNC and TNC locking connectors. The connectors provide optimum 50 $\Omega$  impedance for external wiring or microwave-band and high-speed pulse transfer signals in mobile-communications equipment as well as in GPS applications. VSWR is 1.3 or less from dc to 3 GHz (not including the terminator). \$6.74 per mated pair (1000). **Hirose Electric USA Inc.**, Simi Valley, CA. (805) 522-7958.

**Circle No. 471**



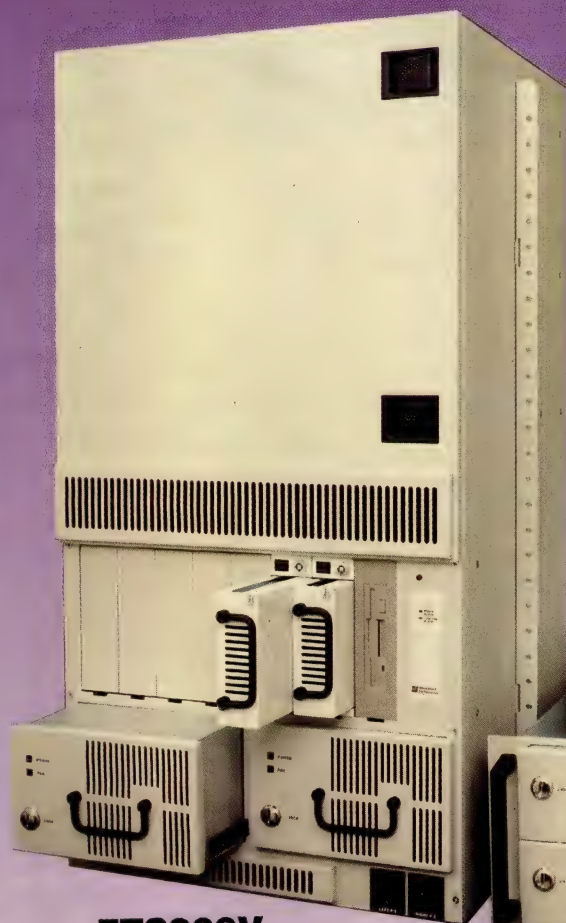
**CONVERTER WORKS  
WITHOUT AC POWER  
OR BATTERIES.**

The synchronous Model 2020-25 RS-232C-to-V.35-interface converter draws all necessary operating power from the RS-232C and V.35 interfaces and, therefore, requires no ac power or batteries. The device suits use with bridges, routers, channel-service units, and other WAN-access devices and supports data rates as fast as 384 kbps. The device has a DB-25 connector on each end and 6 ft of shielded twisted pair in between. The



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**FTS900  
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Drive Bays for the FTS900V

Provisions for up to 5 Drive Bays  
for the FTS900

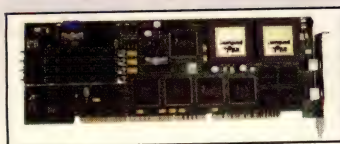
2 Redundant 375w Hot Swappable,  
Load Sharing Power Supplies (AC or DC)

Front Panel Status Indicator

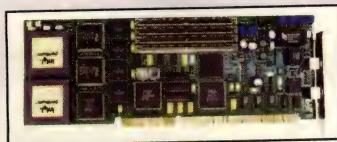
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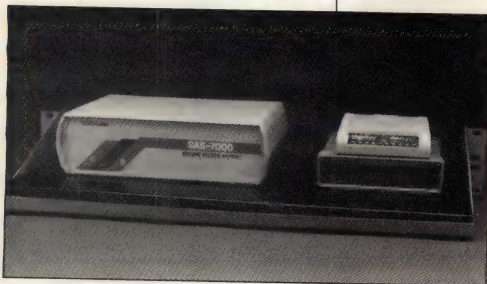
RS-232C end houses surface-mount electronics, and the other end supports V.35 communication, according to the RS-530 standard. A data-communications-equipment/data-terminal-equipment switch lets the device work with different combinations of devices and interfaces. Apart from the switch, the converter requires no user configuration. Price is \$295. **Patton Electronics Co**, Gaithersburg, MD. (301) 975-1000.

**Circle No. 472**

**NOISE DIODES SUIT  
WIRELESS APPLICATIONS.**

The NC302LBL noise diode suits use in wireless applications, such as built-in calibration references in signal-strength meters. The device features a 20- to 35-dB excess-noise ratio and covers 10 Hz to 3 GHz with white Gaussian noise when biased at 8 mA from a >12V-dc supply voltage. The operating temperature range is -55 to +125°C. The device comes in a surface-mount, hermetically sealed ceramic package and costs \$5.95 (10,000). **Noise Com Inc**, Paramus, NJ. (201) 261-8797.

**Circle No. 473**



**▲ SYSTEM PROVIDES  
SECURE ACCESS TO FOUR  
REMOTE USERS.**

The ISAS-4X8 integrated secure-access system comprises four of the company's eight-port SAS-7008 access units, a Security Dynamics SecureID card, a Security

Dynamics ACM-400 access module, and four V.34 modems. The device provides secure access to networks, automatic teller machines, test equipment, and other computer devices. It operates from 110V ac or 48V dc. It provides four users with simultaneous remote access to any of eight devices. The system operates in human- or computer-activated remote-diagnostics methods. Price is \$7890. **Gilltro-Electronics Inc**, Santa Clara, CA. (408) 727-6422.

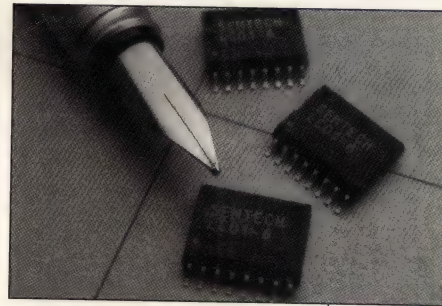
**Circle No. 474**

**FIBER-OPTIC ST CONNECTORS  
PROVIDE FAST  
TERMINATION.**

The ST-compatible Quick Shot ramped bayonet connector comes with a preloaded adhesive and requires one-stage polishing. To terminate Quick Shot, the connector clips into a holder that eliminates the danger of operators burning their fingers when handling a hot assembly. The operator places the holder and connector into an oven to melt the adhesive. Heat indicators on the holder change from blue to bright orange to alert a user when the adhesive is hot and molten. After removing the assembly from the oven, the user inserts a stripped fiber into the connector, which then cools.

The heat indicator returns to blue when the adhesive is cured. An integral clamp on the holder ensures that the fiber remains in position while the adhesive is curing. Price is \$6/unit in moderate quantities. **ITT Cannon**, Santa Ana, CA. (714) 261-5300.

**Circle No. 475**



**▲ VOLTAGE SUPPRESSOR  
PROTECTS COMMUNICATION-  
INTERFACE ICs FROM  
OVERVOLTAGE.**

The LC01-6 transient-voltage-suppressor diode protects high-speed data/telephone-line communication-interface ICs from overvoltages. The device has a transient-power rating of 1500W-pk-pulse power and a maximum clamping voltage of 16V. Capacitance is <50 pF. The diode also protects RS-422 data lines, integrated-services digital-network and ATM interface cards, and cellular base stations and exchanges. The LC01-6 costs \$4.45 (5000). **Semtech Corp**, Newbury Park, CA. (805) 498-2111.

**Circle No. 476**

**INERTIAL-NAVIGATION  
SYSTEM REPLACES EXPENSIVE  
GYROSCOPE SYSTEMS.**

The AX100 DHS attitude-heading reference system provides compass (azimuth), tilt, and rotation information. The system replaces mechanical or fiber-optic gyroscope systems in military and commercial ships, vehicles, and jets. The AX100 EGI inertial-navigation unit has an embedded global-positioning-system (GPS) receiver and provides position, direction, and orientation information. Both products integrate three magnetometers, three accelerometers, and three gyroscopes through a Kalman filtering process. Fil-

ter software allows each magnetometer to counterbalance weaknesses in the other sensors. The magnetometers correct for gyroscope drift, the accelerometers allow for

dead reckoning when GPS signals are lost, and the gyroscopes maintain accurate compass heading in the presence of strong magnetic disturbances. Prices for the AX100 DDS and AX100 EGI start at \$8000 and \$12,000, respectively. **Precision Navigation Inc**, Mountain View, CA. (415) 962-8777.

**Circle No. 477**

**RF POWER MOSFET PROVIDES  
THERMAL STABILITY.**

The 28V MRF160 MOSFET operates at a dc to 500-MHz frequency range. The device suits class A operation and features high thermal stability and low feedback capacitance. The MOSFET offers 400-MHz typical performance at 4W output power, 17-dB gain, and 50% efficiency. It suits use in wide-band, large-signal-output, and driver applications and can withstand 30-to-1 load VSWRs of any phase angle. Price is \$20.93 in small volumes. **Motorola Inc**, Phoenix, AZ. (602) 244-6108.

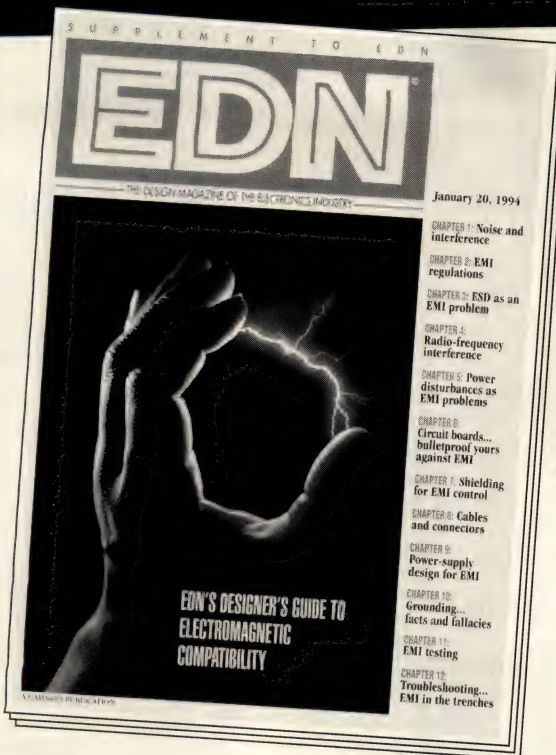
**Circle No. 478**

**SONET VCXOs REACH  
850-MHZ FREQUENCY.**

These ECL-compatible voltage-controlled crystal oscillators (VCXOs) cover the 115- to 850-MHz synchronous-optical-network (SONET) frequency range and come in fixed-frequency models. The devices operate over a -40 to +85°C temperature range and feature



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CIRCLE NO. 26

## SPECIAL SECTION

## Communications Products

$\pm 100$ - to  $\pm 10$ -ppm frequency tolerances, depending on the temperature range. Phase jitter is 10 psec rms max and 5 psec rms typ. Prices range from \$80 to \$145 per unit, depending on the frequency and quantity. **Connor-Winfield Corp**, Aurora, IL. (708) 851-4722.

Circle No. 479

### BAND-REJECT FILTER NOTCHES OUT SIGNALS IN WIDE INTERFERENCE BAND.

The Model F-11249 band-reject filter features a passband of dc to 8.5 GHz and 14 to 14.5 GHz and a reject band of 9 to 12 GHz. The insertion loss is  $< 1$  dB in the passband, and the rejection is  $> 45$  dB in the reject band. Prices start at \$295 in small quantities. **RLC Electronics Inc**, Mount Kisco, NY. (914) 241-1334.

Circle No. 480



### ▲ DEVICE FINDS TRANSMISSION IMPAIRMENTS.

The 188T transmission-line test set tests and troubleshoots leased lines and dial-up circuits. The device meets or exceeds IEEE 753, Bell pub41009, and Consultative Committee on International Telephone and Telegraph standards. The menu-driven system includes a rotary selector switch and a pushbutton keypad. Analytical functions include TIMS, impulse, hits, jitter, and peak-to-average-ratio measurements. The system also incorporates dialing and optional RS-232C capabilities. TIMS mode lets you transmit and

receive 20-Hz to 50-kHz signals. The test set can measure signals from  $+10$  to  $-60$  dBm and detects 10- to 100-dBm noise levels with 1-dBm resolution. The device has a dual Bantam miniature phone jack and an RJ45 modular jack. A dialing generator activates remote two- or four-wire responders, rendering a dual-tone multifrequency, dial-pulse, or multifrequency dial signal. Price is \$2975. **American Reliance Inc**, Arcadia, CA. (818) 303-6688.

Circle No. 481

### PLL FREQUENCY SYNTHESIZER HAS ON-CHIP ADC.

The MC145173 single-chip PLL frequency synthesizer includes a four-wire serial interface for use in AM-FM broadcast receivers, long- and short-wave receivers, VHF scanners, and other RF applications using the 550-kHz to 130-MHz bandwidth. The device includes a 6-bit on-chip ADC that lets a user monitor two voltage levels in a radio application, a 22-stage frequency counter that accepts two IF signals for a seek or scan function on radio receivers, and a current-source/sink phase-detector output. The MC145173 comes in a 24-lead, plastic, small-outline, gull-wing package and costs \$2.04 (5000). **Motorola, MOS Digital-Analog IC Division**, Austin, TX. (800) 422-6323.

Circle No. 482

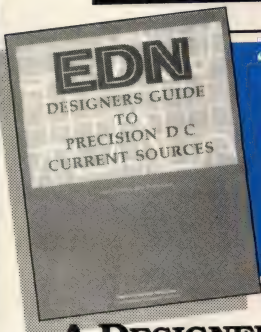
### OPTICAL/ELECTRICAL PLUG-IN MODULE.

Optical/Electrical Plug-In Module (Option 05) is an enhancement for the CTS 710 SONET and CTS 750 SDH test sets. The Option 05 plug-in module handles 0-dBm measurements for data rates to 622 Mbps at the 1550-nm wavelength. Key upgrades for Option 05 include a set of pointer sequences, overhead byte functions, a 45-day record that extends coverage of graph and test history records, and a comprehensive AutoScan display that presents mixed tributary structures and detailed status information on all scanned channels. Option 05 for the CTS 710 SONET test set costs \$20,900; Option 05 for the CTS 710 model costs \$15,900; existing customers receive upgrades for free. **Tektronix Measurement Group, Literature Distribution Center**, Pittsfield, MA. (800) 426-2200, ask for code 405.

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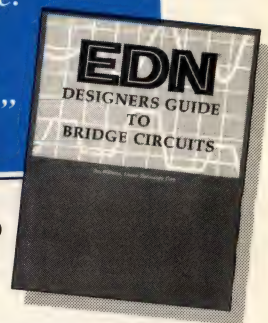


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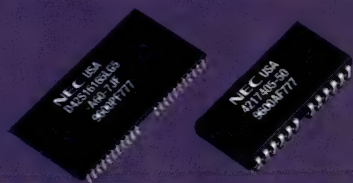
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μPD42S16165L		1Mb x 16		4K
μPD42S18165L		1Mb x 16		1K
μPD42S16405	5.0V	4Mb x 4	20/25/30ns	4K
μPD42S17405		4Mb x 4		2K
μPD42S17805		2Mb x 8		2K
μPD42S16165		1Mb x 16		4K
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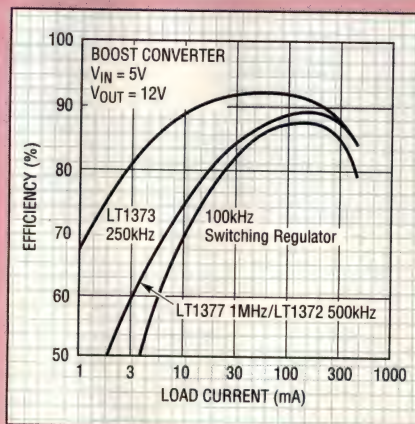


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# Regulator generates as many as four voltages

D HAYDEN, HAYDEN ELECTRONICS DESIGN, SAN DIEGO, CA

The inexpensive switching regulator in Fig 1 provides as many as four voltages using a single quad comparator. The circuit can implement two positive regulated supplies and two semiregulated negative supplies that use a charge-pump technique. Fig 1's circuit, which costs \$4.48 in moderate volumes, shows three of the four possible output voltages,  $\pm 9\text{V}$  and  $150\text{V}$ . You can add a  $-150\text{V}$  supply using the same charge-pump techniques as the  $-9\text{V}$  supply. Output current of the  $+9\text{V}$  supply is nominally  $10\text{ mA}$ . The  $-9\text{V}$  can typically provide  $5$  to  $10\text{ mA}$  and tracks the positive supply well. The  $150\text{V}$  supply can output around  $200\text{ }\mu\text{A}$ . Four AA batteries provide a supply voltage from  $4$  to  $6\text{V}$ . An RC time constant on power-up delays the comparator's supply voltage to prevent the switching transistors from turning on before the reference voltage is stable. An external clock source of  $31.25\text{ kHz}$  swings between circuit ground and the battery level.

For the positive  $9\text{V}$  supply in Fig 1, comparator  $\text{IC}_{1\text{D}}$  senses the  $9\text{V}$  level and compares it with the  $1.2\text{V}$  reference. When the  $9\text{V}$  output is low, the comparator output goes to ground. The  $1\text{N}4148$  diode holds the inverting diode input to  $\text{IC}_{1\text{C}}$  to  $0.7\text{V}$ , and the noninverting input is the clock signal divided by 2. (This signal swings from one-half of the battery voltage to ground.)  $\text{IC}_{1\text{C}}$ 's output, which  $\text{R}_1$  pulls up to the battery voltage, then switches at the clock frequency.

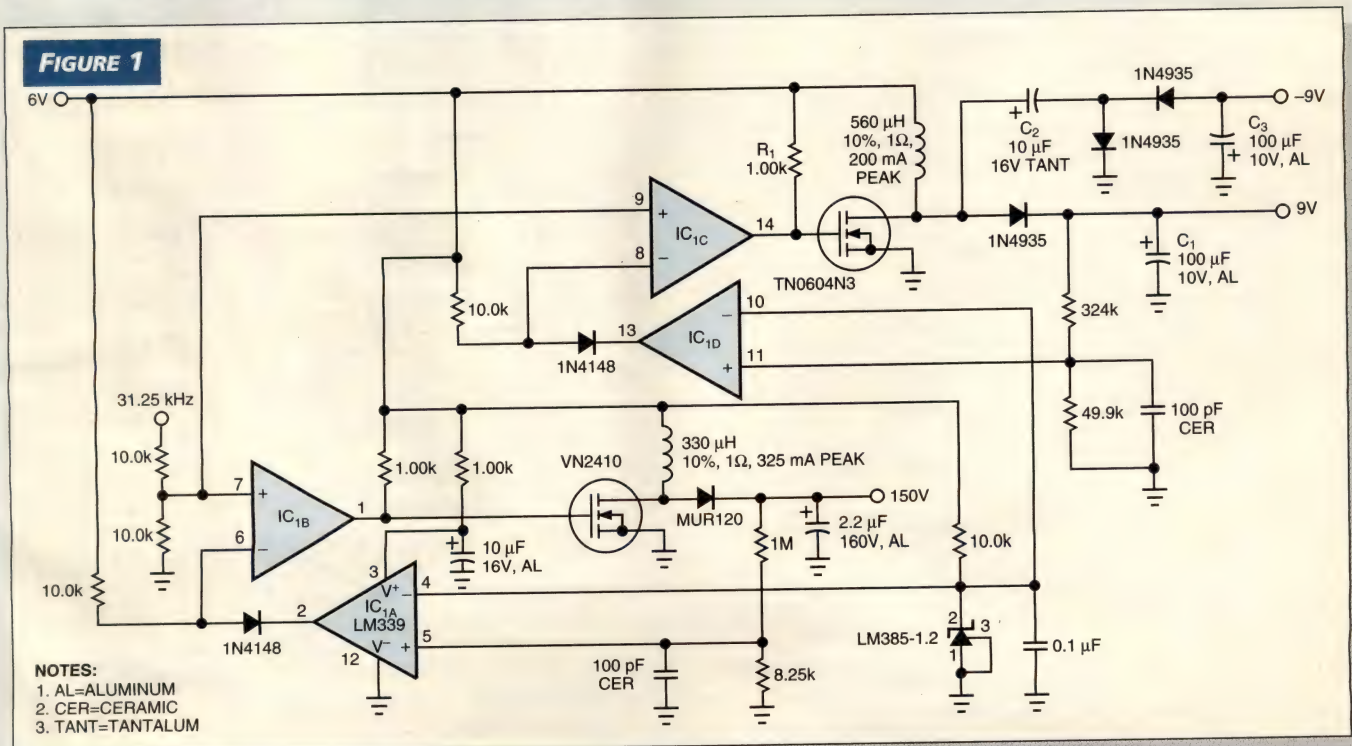
Current switches through the inductor to charge up  $\text{C}_1$  until the  $9\text{V}$  output rises enough to set the output of  $\text{IC}_{1\text{D}}$  high. With  $\text{IC}_{1\text{D}}$  high and equal to the battery voltage, the circuit blocks the divided clock signal from  $\text{IC}_{1\text{C}}$ , leaving  $\text{IC}_{1\text{C}}$ 's output low. You must choose the size of the inductor so that it doesn't saturate with the maximum drive on-time and maximum battery voltage.

The waveform at  $\text{Q}_1$ 's drain is a square wave that swings from  $9.7\text{V}$  to ground. To generate the  $-9\text{V}$  output, the circuit couples this signal through  $\text{C}_2$  and clamps it to ground. The waveform at the junction of the two  $1\text{N}4935$  diodes is a square wave swinging from  $+0.7$  to  $-9.0\text{V}$ .  $\text{C}_3$  charges during the negative swings to about  $-8.3\text{V}$ .

The positive  $150\text{V}$  supply works in the same way as the  $9\text{V}$  supply but with different components to provide the higher-voltage output. The circuit's measured efficiency is between  $75$  and  $80\%$  over the battery voltage range. You can increase the circuit's efficiency if you can tolerate higher component costs. Also, if you need only two output voltages, you can use a dual comparator, such as the  $\text{LM}393$ . (DI #1742)

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This circuit generates three output voltages: two positive regulated supplies of  $9$  and  $150\text{V}$  and a semiregulated  $-9\text{V}$  supply.



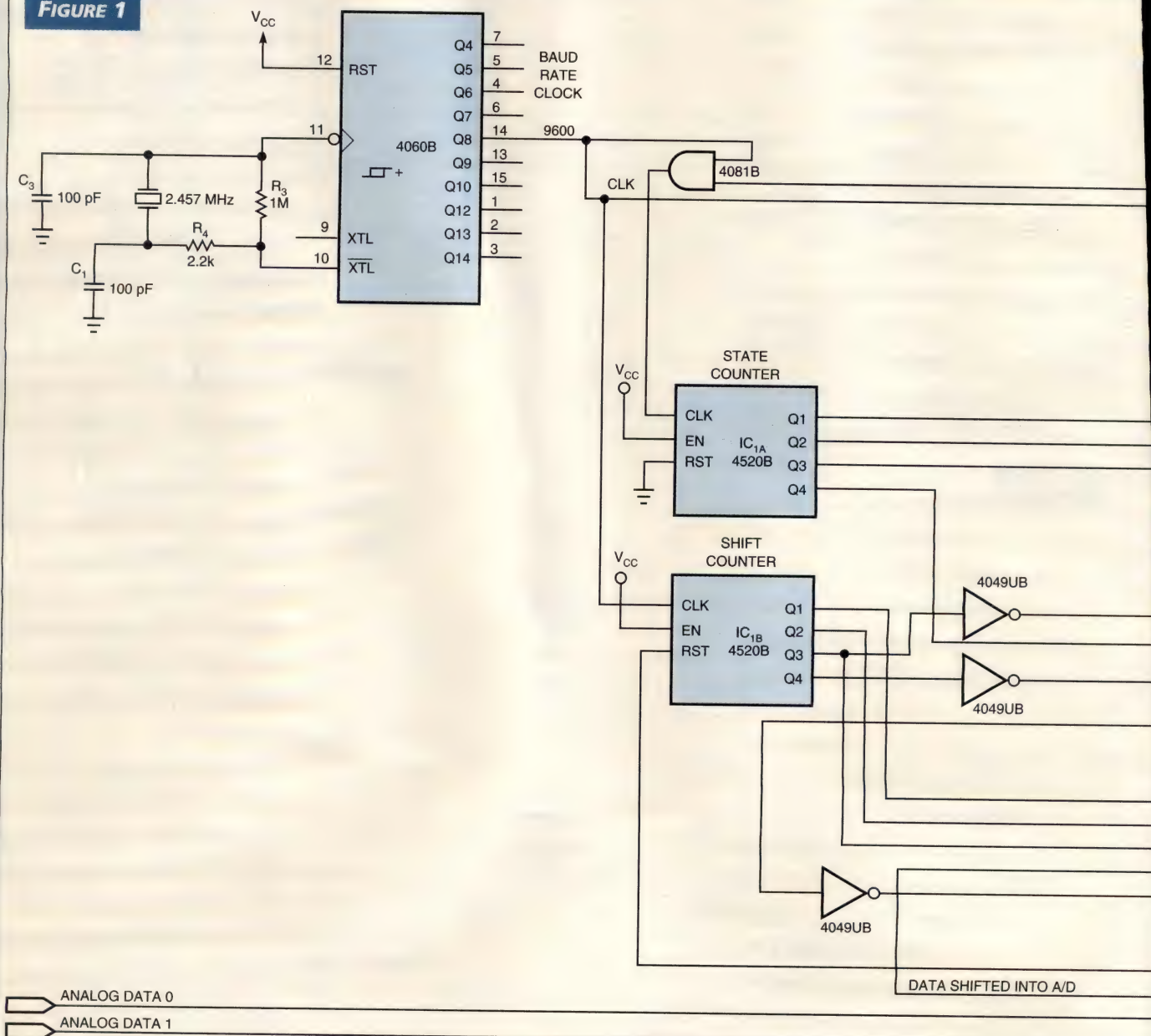
## Data-acquisition system draws less than 10 mW

**NOOR KHALSA, EG&G, LOS ALAMOS, NM**

The data-acquisition system in Fig 1 draws approximately 2.2 mA at 3.6V. It consists of a state machine that converts the synchronous serial data from the A/D-converter chip into a standard baud rate framed with start and stop bits for easy interface with a computer's COM port. The counter IC<sub>1A</sub>

controls the state machine; IC<sub>2</sub> decodes the states. The first step is to program the A/D converter by shifting four bits into it. The counter IC<sub>1B</sub> counts the four bits; these bits then shift from the analog-multiplexer IC<sub>5</sub> into the A/D converter.

The second state of the state machine sends a start bit to

**FIGURE 1**

**This data-acquisition circuit draws less than 10 mW of power and provides easy interface to a computer's COM port.**

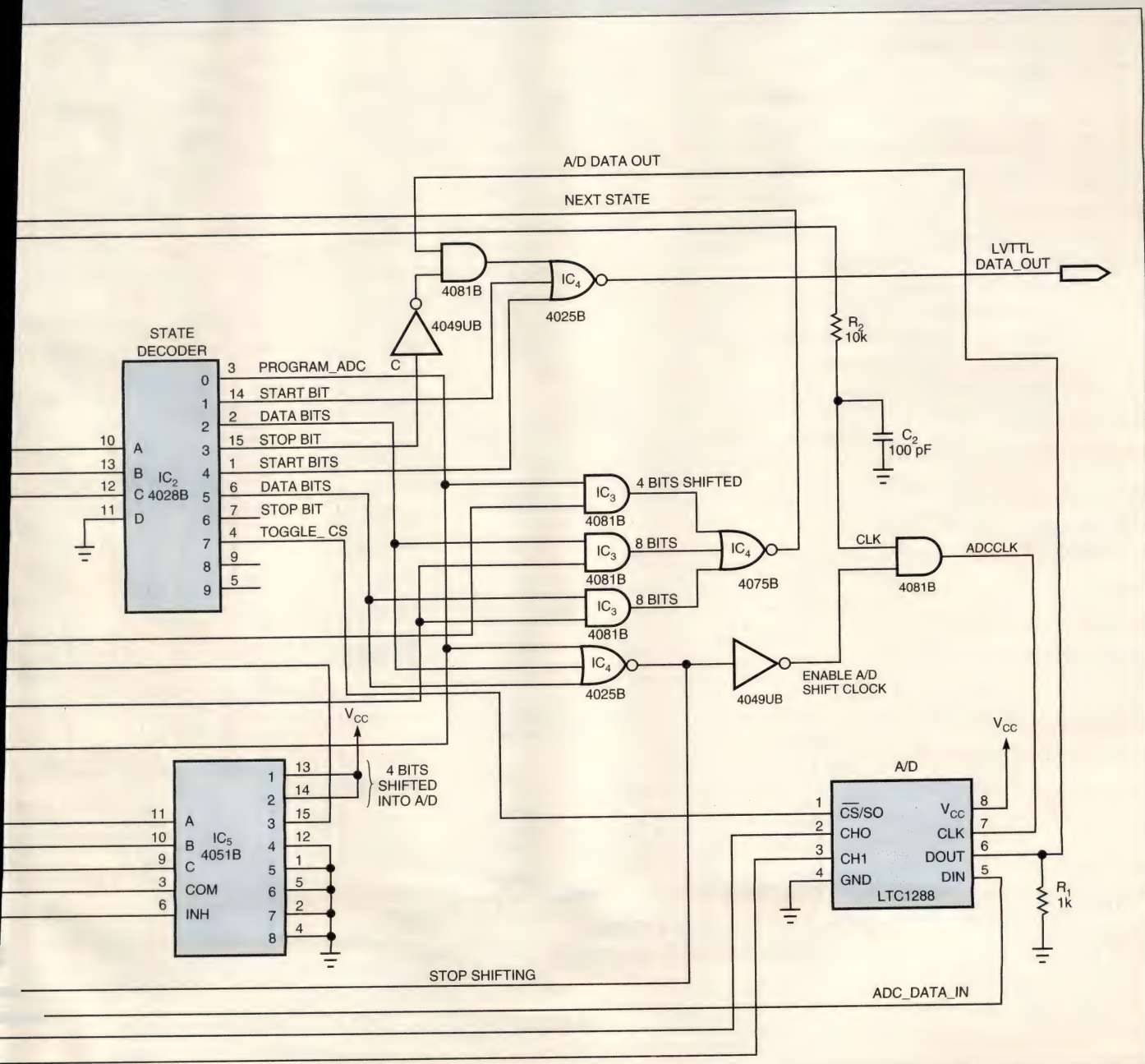


the data\_out line. The third state shifts out the last eight bits from the 12-bit A/D converter. Counter IC<sub>1B</sub> counts the eight bits, and the fourth state of the state machine inserts a stop bit. The sixth state starts another serial frame by inserting a start bit. Then, the circuit clocks the A/D converter eight more times, and the converter shifts out the last four data bits and four zeros. The A/D converter then receives another stop bit and, finally, a chip-select toggle to initiate another conversion cycle.

The logic at gates IC<sub>3</sub> and IC<sub>4</sub> simply determines whether the second counter IC<sub>1B</sub> needs to count four bits or eight before proceeding to the next state. Pin 7 of counter IC<sub>1A</sub> produces a read operation of the second A/D-converter channel on every other pass of the state machine by toggling the channel-select bit the analog multiplexer shifts into the converter. (DI #1727)

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# Rotary controller positions stepping motor

TG BARNETT AND ME ROSENBERG, DEPARTMENT OF PHYSIOLOGY,  
QUEEN MARY AND WESTFIELD COLLEGE, LONDON, UK

The circuit in Fig 1 uses a servo potentiometer, as opposed to a rotary switch or encoder, to provide the necessary drive pulses for a stepping motor. This motor positions a pointer by the rotation of a manual control. The circuit must be precise, allow a rapid response, and be simple to use. (This circuit was part of a complex apparatus used for a series of physiological tests.) Another requirement is that the control had to be a small, handheld, battery-operated device.

The angle of the pointer needs to be set at greater than 10 minutes of arc, resulting in the choice of a motor and drive system with 4000 steps per complete revolution in a system with logic pulses for step and direction control. The direction of rotation of the motor must mimic that of the potentiometer. Also, the variable stepping rate (1, 10, and 1000 times/sec) must be related to the number of degrees the potentiometer turns. That is, the maximum step rate should result when the potentiometer turns fully either clockwise or counterclockwise.

$R_1$  provides 180° of electrical and mechanical rotation. The device is spring-biased, so it returns to a central position when you don't actively rotate it. The circuit applies the voltage at  $R_1$ 's wiper to a series of comparators configured as double-ended limit detectors. A chain of tapped resistors provides reference voltages  $W_A$ ,  $W_B$ , and  $W_C$  for the three limit detectors. The outputs of these detectors control a programmable crystal oscillator (PXO) that generates the stepping

pulses. One additional single-ended comparator provides direction control. Four AA batteries provide a supply voltage of 5V.

The outputs of the detectors depend on the position of  $R_1$ . When  $R_1$ 's position is between 54 and 126°, the output of NAND gate 8 is low, which disables the oscillator through its reset pin. On either side of these positions, the output of NAND gate 8 is high, which enables the oscillator. Then, according to  $R_1$ 's position, the outputs of gates 9, 11, and 13 go low. The result is respective oscillator output frequencies of 1, 10, and 1000 Hz as the user turns the potentiometer toward either end stop. Note that the output of NAND gate 14, which comparator 7 drives, controls the direction of motor rotation. Comparator 7 changes logic level at the 90° position.

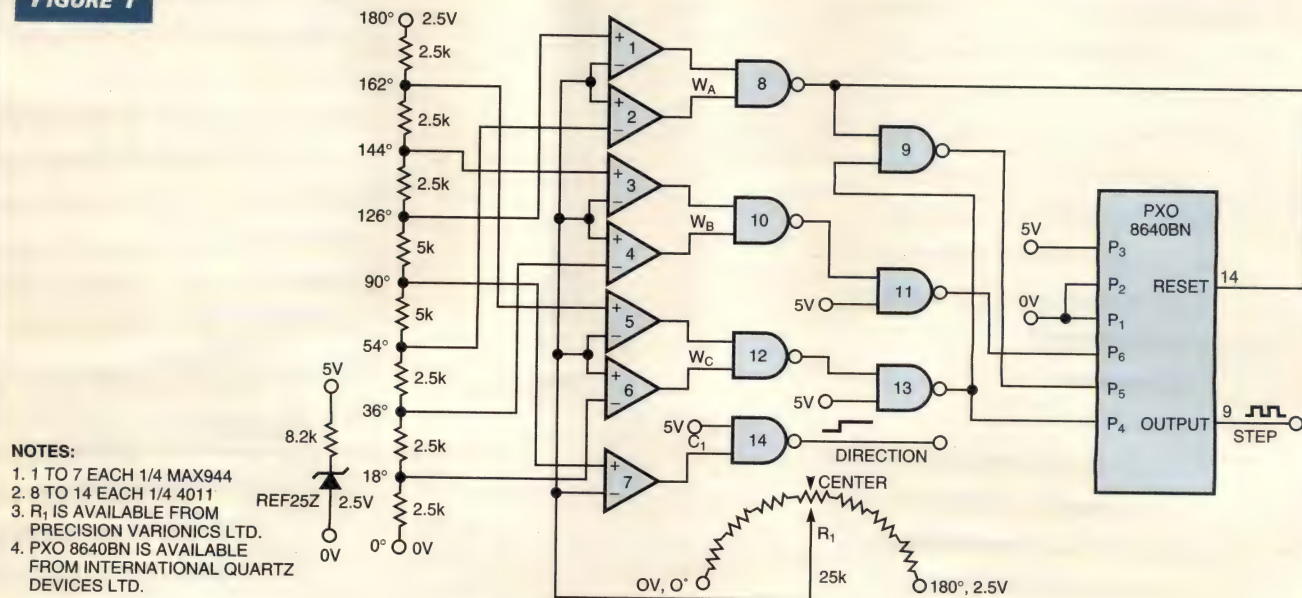
You can add or remove comparators for a different sequence comparison. If you increase the number of comparators, you should buffer the reference and potentiometer wiper voltages. Also, you can program the PXO 8640BN using controls  $P_1$  to  $P_6$  to oscillate at 57 frequencies or use the oscillator merely as a divider driven from an external frequency source. (DI #1739)

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(continued on pg 96)

FIGURE 1



Servo potentiometer  $R_1$  controls a bank of limit detectors which, in turn, control the speed and direction of a stepper motor.



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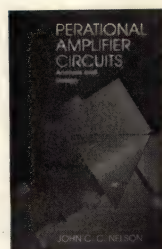
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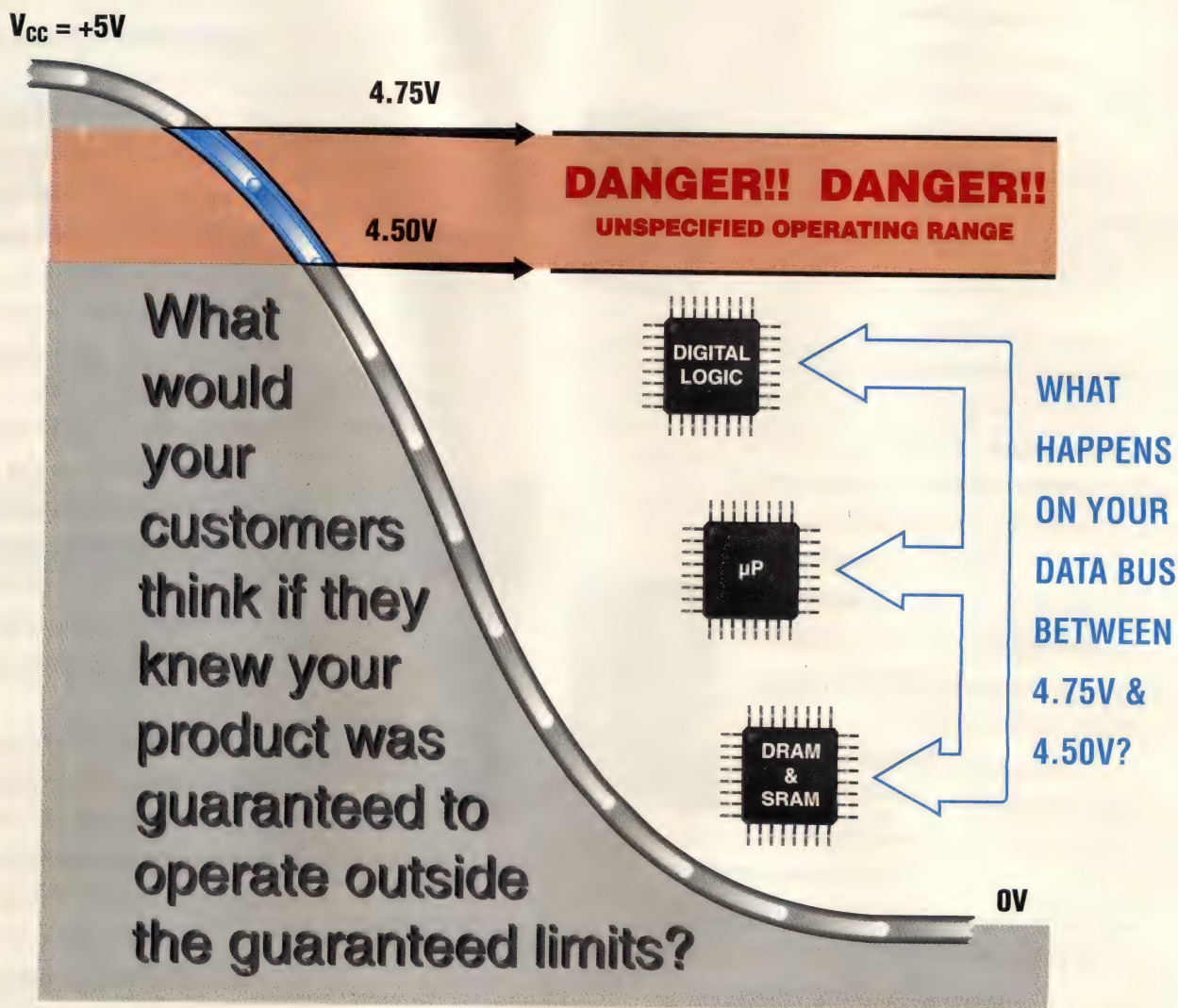
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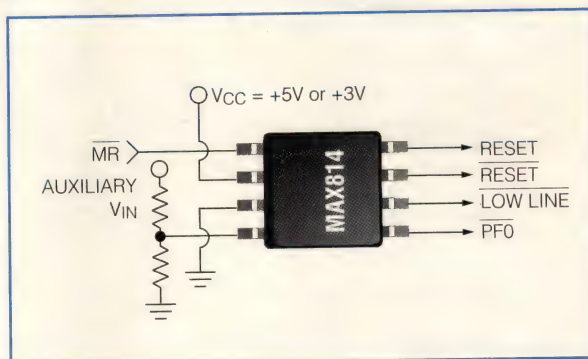
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# Circuit loads eight-channel DAC from PC port

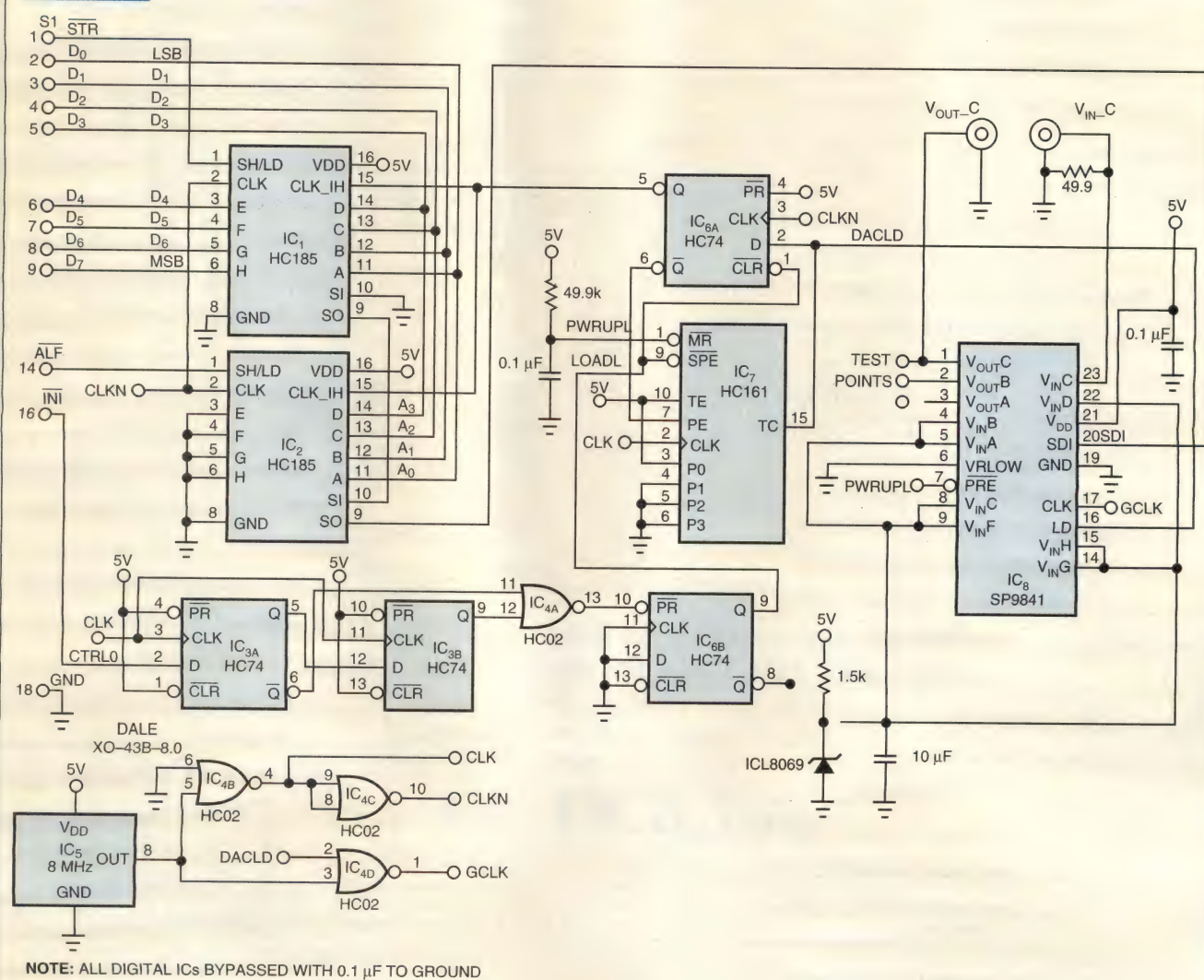
DANIEL SEGARRA, SIPEX CORP, BILLERICA, MA

**BBS** The circuit in Fig 1 loads 4 address bits and 8 data bits into IC<sub>8</sub>'s 8-bit octal, two-quadrant multiplying DAC from a PC parallel port. Initially, the circuit loads the desired data on the D<sub>0</sub> through D<sub>7</sub> pins of the parallel port into shift register IC<sub>1</sub> when the parallel port's STR pin goes low. Next, the circuit loads the desired address from the port's D<sub>0</sub> through D<sub>3</sub> pins into register IC<sub>2</sub> when the port's ALF pin goes low.

The data shift from the registers into the DAC when the

INI pin (CTRL0) of the parallel port goes high. The circuit formed by IC<sub>3</sub> and IC<sub>4A</sub> synchronizes INI with the on-card clock. IC<sub>6B</sub> performs an inversion and generates a pulse at LOADL, which goes low for the duration of one clock period each time INI goes high. LOADL is synchronous with the on-card clock signal, CLK. The LOADL signal loads binary 1 into counter IC<sub>7</sub>, and simultaneously drives the clock-inhibit pins of shift registers IC<sub>1</sub> and IC<sub>2</sub> low via IC<sub>6A</sub>. This action puts the registers in serial-out mode.

FIGURE 1



This circuit loads 4 address bits and 8 data bits into an 8-bit octal, two-quadrant multiplying DAC from a PC parallel port.

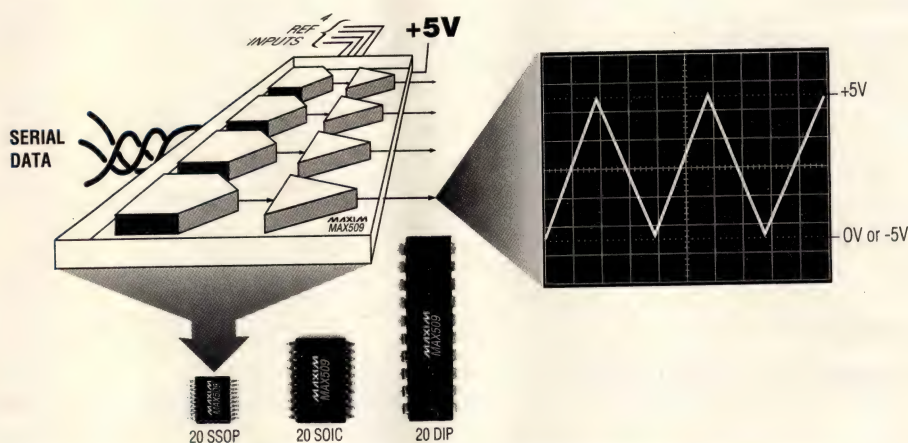


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IC<sub>5</sub>'s oscillator and the remaining gates of IC<sub>4</sub> produce three clock signals: CLK, CLKN, and GCLK. CLK and CLKN are out of phase, and GCLK is a gated clock in phase with CLK. Data shift out of the registers on the rising edge of CLKN and shift into the DAC on the rising edge of CLK. Initially, the first of four leading zeros appears at the SO pin of IC<sub>2</sub>. A total of 15 CLKN edges are necessary to shift out the remaining zeros followed by A<sub>3</sub> through A<sub>0</sub> and D<sub>7</sub> through D<sub>0</sub>, in that order. During this time, IC<sub>7</sub> counts from its loaded state of binary 1 to 15.

Note that the counter can't begin counting until the LOADL signal goes high. Thus, the DAC misses the first two leading zeros. The DAC's internal register simply shifts out the last two leading zeros by the time the 14th rising edge of CLK occurs. This edge also produces the DACLD signal—the counter's ripple carry out—that disables GCLK, strobes the load pin of the DAC, and causes the inhibit pin of the shift registers to go high. The cycle is now complete, and the circuit can load new address and data bits from the parallel port.

The program in Listing 1 accepts an address (1 through 8) and data (0 through 255) in decimal format and sends the information to the DAC. Addresses 1 through 8 correspond to converters A through H, respectively. The output is as follows:  $V_{OUT} = (\text{data}/128) \times 1.5V$ . We found that, for the IBM PC/XT, the LPT1 port address was 3BCH (Data Register 3BCH and control register 3BEH). You can download the listing from EDN BBS /DI\_SIG #1738. (DI #1738) **EDN**

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## LISTING 1

```

PROGRAM TO LOAD DAC FROM PARALLEL PORT
' This program accepts an address (1 through 8) and data (0 through 255)
' in decimal and sends them to the DAC. Address's 1 through 8 will
' correspond to converters A through H respectively. The output will be
' Vout=(data/128)*1.5 volts.

' We found that for out IBM PC/XT the LPT1 port address was 3BCH
' (Data Register 3BCH and control register 3BEH).

DIM lsb AS INTEGER
DIM msb AS INTEGER
DIM datareg AS INTEGER
DIM cntlreg AS INTEGER
DIM n AS INTEGER
datareg = &H3BC: cntlreg = &H3BE
CLS

n = 0
DO WHILE n = 0
  DO
    test$ = ""
    INPUT "Enter Address (1 through 8): ", lsb
    IF lsb < 1 OR lsb > 8 THEN test$ = "false"
    IF test$ = "false" THEN PRINT "Please enter a valid address.": PRIN
    LOOP UNTIL test$ <> "false"

  DO
    test$ = ""
    PRINT
    INPUT "Enter Data (0 through 255 in decimal): ", msb
    IF msb < 0 OR msb > 255 THEN test$ = "false"
    IF test$ = "false" THEN PRINT "Please enter valid data. ": PRINT
    LOOP UNTIL test$ <> "false"

    OUT cntlreg, &H3 'set both latch clocks low
    OUT datareg, &H0 + msb 'send most significant byte to port
    OUT cntlreg, &H2 'clock IC1

    OUT cntlreg, &H0 + lsb 'send least significant byte to port
    OUT datareg, &H0 'clock IC2
    OUT cntlreg, &H4 'enable IC7, set IC1 & IC2 to serial out

    PRINT : PRINT "Strike spacebar to enter new data or Q to quit."
    DO
      XS = INKEY$
      IF UCASE$(XS) = "Q" THEN n = 1
      LOOP UNTIL XS = " " OR UCASE$(XS) = "Q"
    LOOP
  
```

## Resistance calculator yields precise values

DAVID KIRKBY, DEPARTMENT OF MEDICAL PHYSICS, UNIVERSITY COLLEGE LONDON, LONDON, UK.



For times when the nearest preferred resistor value isn't close enough to the desired value, a program comes in handy. (You'll find the executable ZIPfile and several source-code files for the program in EDN BBS /DI\_SIG #1740.) The program finds all combinations of two series or parallel connected resistors, within a specified tolerance of the required value, using only preferred values from the E6, E12, E24, and E96 ranges (6, 12, 24, and 96 different values per decade).

The program, which is written in C and runs on the PC, has four arrays that contain the preferred values of each range. The two smallest arrays are listed below.

double e6[6] = 1.0, 1.5, 2.2, 3.3, 4.7, 6.8;

double e12[12] = 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2;

The program has a simple main loop that requests the following information from the user: the value of the resistor required (such as 1234Ω); the range (for example, E24); the

minimum (such as 10Ω) and maximum (for example, 2.2 MΩ) resistor available in the range; whether you plan a series (S), parallel (P), or both (B) connection; and, finally, the accuracy required (for example, 0.5%). The program then lists all combinations that meet or exceed the accuracy requirement.

For these given example values, the best series combination would be 33 and 1200Ω, giving 1233Ω. However, a better combination is 1.3 kΩ in parallel with 24 kΩ, giving 1232.2Ω.

The program requires ANSI.SYS or equivalent installed on the PC for screen control. Although the program was written for resistors, you can also use it for inductors and capacitors. For capacitors, you need to transpose the meaning of series and parallel. (DI#1740) **EDN**

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DESIGN IDEAS

## Algorithm evaluates complex fractions

PAUL JOHNSON, HEWLETT-PACKARD, ESCONDIDO, CA

The following algorithm uses rectangular-to-polar conversion to evaluate a complex fraction (one that includes imaginary numbers). The algorithm is most convenient when you can perform the rectangular-to-polar-coordinate and polar-to-rectangular-coordinate conversions using a calculator such as an HP 11C. You can reduce all the necessary steps to two keystrokes or, if the calculator is programmable, to one program step. When computing transfer functions and Bode plots, you can determine the gain and phase at the end of step 4 before doing step 5.

The algorithm steps are as follows:

1. Reduce each complex term to a rectangular-coordinate number of the form  $x+yi$ .
2. Convert each term from a rectangular-coordinate number of the form  $x+yi$  to a polar-coordinate number of the form  $(r,\theta)$ .
3. Calculate the  $r$  of the resulting polar coordinate by calculating the product of the  $r$ 's in the numerator divided by the product of the  $r$ 's in the denominator.
4. Calculate the  $\theta$  of the resulting polar coordinate by computing the sum of the  $\theta$ 's in the numerator minus the sum of the  $\theta$ 's in the denominator.
5. Convert the resulting polar coordinate number of the form  $(r,\theta)$  to a rectangular coordinate number of the form  $x+yi$ .

Eqs 1 and 2 show these five steps:

$$\frac{1+i}{1-i} = \frac{(\sqrt{2}, 45)}{(\sqrt{2}, -45)} = \left( \frac{\sqrt{2}}{\sqrt{2}}, 45 - (-45) \right) = (1 \text{ at } 90^\circ) = i \quad 1$$

$$\frac{(3+5i)(1+7i)}{(3+i)(4+i)} = \frac{(5.83, 59)(7.07, 81)}{(3.16, 18)(4.12, 14)} = \quad 2$$

$$\left( \frac{5.83 \cdot 7.07}{3.16 \cdot 4.12}, 59 + 81 - (18 + 14) \right) = (3.17 \text{ at } 108^\circ) = 1 + 3i$$

The following formulas define the relationship between the rectangular and polar coordinates:

$$x = r \cos \theta$$

$$y = r \sin \theta$$

$$x^2 + y^2 = r^2$$

(DI #1743)

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# DESIGN NOTES

## Micropower Buck/Boost Circuits, Part 1: Converting Three Cells to 3.3V\* – Design Note 109

Mitchell Lee

Two combinations of cell count and output voltage are to be strictly avoided: three cells converted to 3.3V and four cells converted to 5V. These combinations are troublesome because no ordinary regulator (boost, buck or linear) can accommodate a situation where the input voltage range overlaps the desired output voltage.

This design note presents four circuits capable of solving the 3-cell dilemma. Design Note 110 will discuss 4-cell, 5V circuits. The LT<sup>®</sup>1303 and LT1372 high efficiency DC/DC converters are used throughout, giving a fair comparison of each topology's efficiency. The LT1303 is optimized for battery operation and includes a low-battery detector which is required to implement one of the topologies. The LT1372

500kHz converter is used for compact layouts at higher current levels.

You can expect 200mA output from LT1303 based circuits and 300mA from the LT1372 circuit without modification. All of the circuits feature output disconnect; in shutdown the outputs fall to 0V. The input range of LT1303 based converters extends well beyond the 3-cell source shown. These function at 1.8V, and although not fully characterized for efficiency, can accept inputs of up to 10V. The LT1372 converter operates from 2.7V to 10V.

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\*For 4-cell to 5V buck/boost circuits, see Design Note 110.

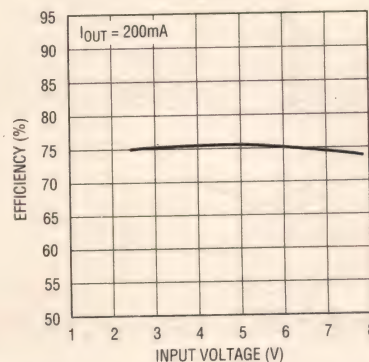
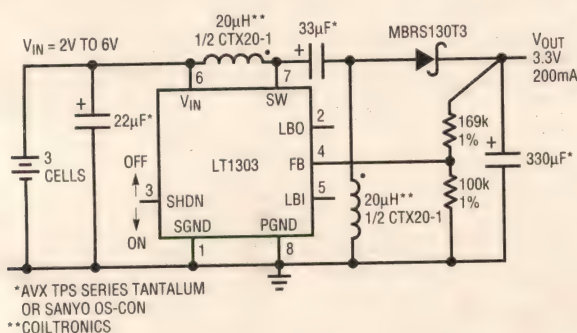


Figure 1. 3-Cell to 3.3V SEPIC

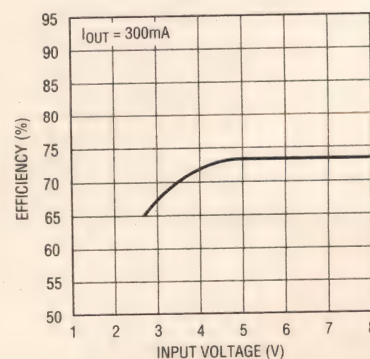
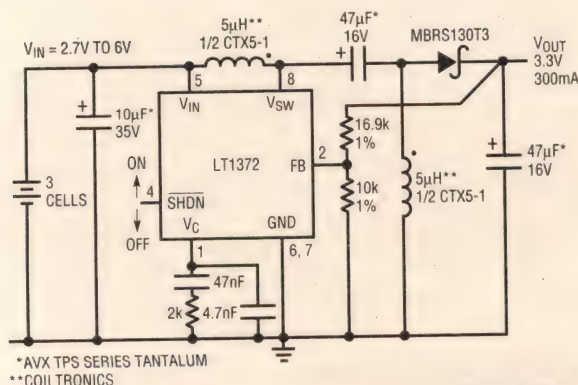


Figure 2



The circuits in Figures 1 and 2 are based on the SEPIC (Single-Ended Primary Inductance Converter) topology. Although not stellar, the efficiency is quite consistent over a wide input voltage range. Peculiar to the SEPIC topology is its use of two inductors. These, however, are wound together on a single core and consume no more space than a simple 2-terminal inductor of similar rating. A wide selection of stock 2-winding, 4-terminal inductors are available from Coiltronics and other magnetics vendors.

Peak efficiency improves in Figure 3 using a bipolar buck/boost topology. This circuit is essentially a boost converter with a linear post regulator. For  $V_{IN} < V_{OUT}$ , the LT1303 boosts the input driving the bipolar emitter just high enough to maintain the desired output voltage—the transistor is saturated. For  $V_{IN} > V_{OUT}$ , the LT1303 drives the emitter to a value just higher than the *input voltage* sufficient to develop the base current necessary to support any load current. In this condition the transistor serves as a linear post regulator, cascoding the output of

the boost converter and dissipating power as would any linear regulator.

Highest peak efficiency is obtained with the circuit in Figure 4 using a MOSFET buck/boost converter. For  $V_{IN} < V_{OUT}$ , the circuit operates as a boost converter and the MOSFET, driven by the LT1303's low-battery detector/amplifier, is held 100% ON. The output voltage is developed and controlled by the boost converter.

For  $V_{IN} > V_{OUT}$ , the boost function can no longer control the output voltage and it begins to rise. Staggered feedback (R3, R4, R5) allows the low-battery detector/amplifier to take control using the MOSFET as a linear pass element. Because the MOSFET requires no base drive, and because it has such a low ON resistance, the efficiency peaks at well over 90%. Furthermore, the efficiency peak occurs in the vicinity of a NiCd's nominal terminal voltage of  $3 \times 1.25 = 3.75V$ , right where the efficiency is needed most.

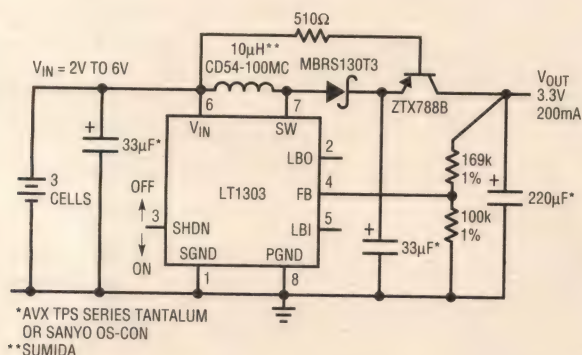


Figure 3. 3-Cell to 3.3V Bipolar Buck/Boost

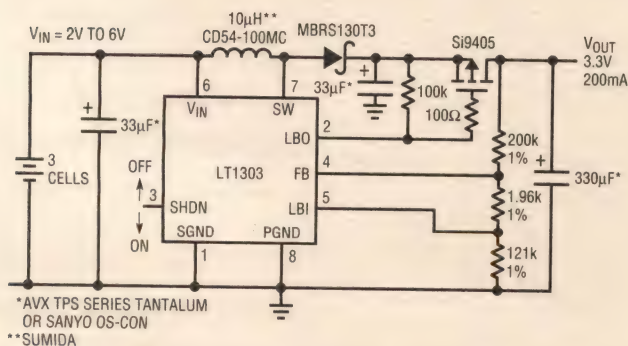
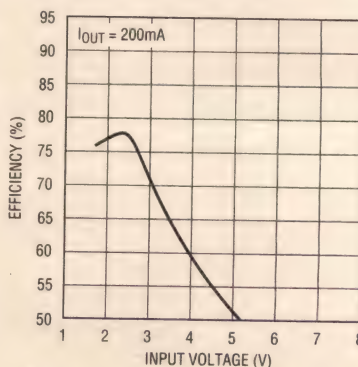
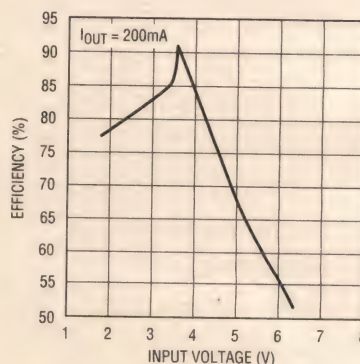



Figure 4. 3-Cell to 3.3V MOSFET Buck/Boost



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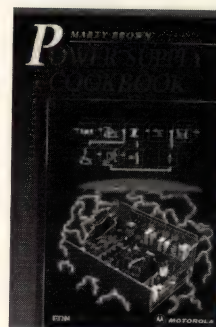
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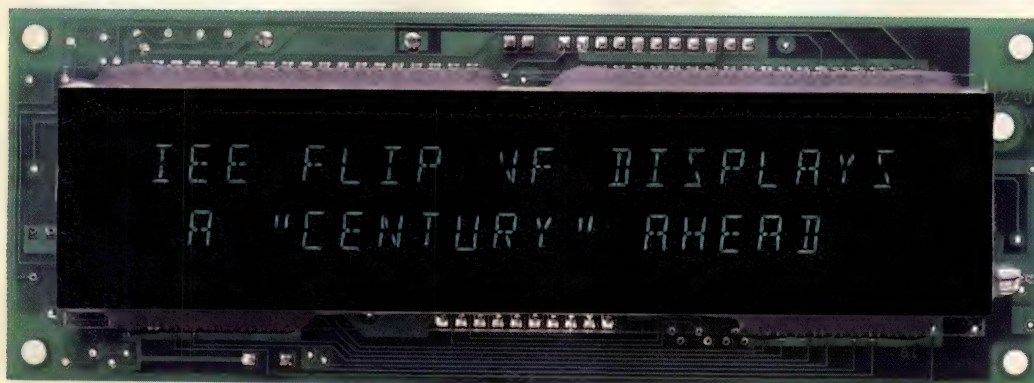
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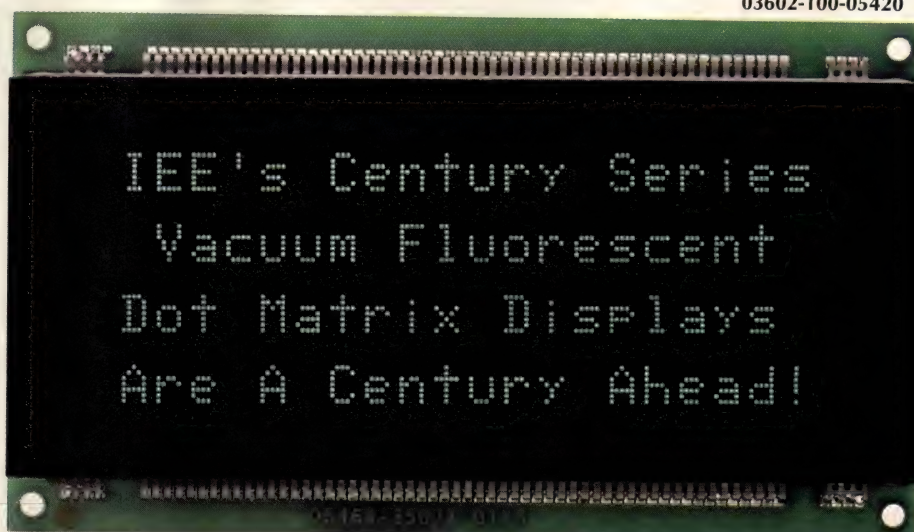
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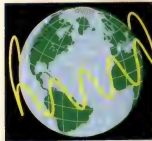
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03602-124-09420	5x7 dot matrix	4x20	9mm	7.75"	3.40"	1.00"	1300mA
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COMMUNICATIONS  
SPECIAL ISSUE

# Use your DSO to measure elusive waveform variations

ROBERT WITTE, HEWLETT-PACKARD CO

Whether analog or digital, all general-purpose oscilloscopes perform the same basic functions. Any scope can measure simple, stable waveforms, such as sine waves or square waves, whose frequency content falls within the scope's bandwidth. Signal variations or transient signals, however, bring out the differences among scopes. If you have a digital storage oscilloscope (DSO), you can use it most effectively if you learn how to take advantage of its strengths and minimize the effects of its shortcomings. If you plan to buy a scope, this information can help you to identify the instrument best suited to your needs.

Ideally, a digital scope samples continuously at a very high rate, so that it never misses anything. In other words, the scope should never stop sampling and should sample so fast that the sample rate is not an issue. Fig 1a shows this ideal situation.

Practical DSOs have a finite sample rate; moreover, they pause after each acquisition to process the acquired samples for display on the screen (Fig 1b). The scope's sampling system determines the sample rate; faster sampling systems cost more. The time that the scope takes to process the acquired samples and prepare for the next acquisition is called dead, or blind, time. The dead time depends on the required amount of data processing and the computational power of the  $\mu$ P or ASIC that crunches the data.

Fig 1b shows the dead time as relatively short—about the

The subtleties of how your DSO works can be just as important as the "banner" specs. The time you spend learning about the instrument's performance details can help you to spot waveform anomalies that you never suspected.

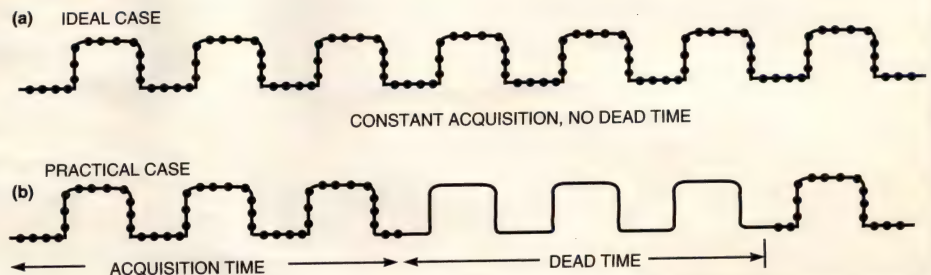
same duration as the acquisition time. The actual situation is usually much worse; the dead time can be orders of magnitude longer than the acquisition time. Another way to quantify this behavior is as a duty cycle—the ratio of acquisition time to total time. The duty cycle, which varies greatly among

scope models and also depends on the scope's sweep speed, can be surprisingly small—sometimes less than 0.0001% when a scope with a long dead time operates at a fast sweep speed.

## Update rate measures efficiency

Another way to represent dead time is via the display-update rate, expressed in samples/second or waveforms/second. Think of the display-update rate as a measure of how efficiently a scope converts its maximum sample rate into displayed points. For example, the HP 54600B, a 100-MHz-bandwidth scope with a very fast display-update rate, has a maximum sample rate of 20M samples/sec but a maximum

FIGURE 1



The ideal situation for scope sampling is a fast sample rate and no dead time (a). The real situation for scope sampling includes a significant dead time between acquisitions (b).



## MEASURING WAVEFORM VARIATIONS WITH DSOs

display-update rate of 1.5M samples/sec. So, when operating at its fastest sample rate, even this very fast scope can convert only 7.5% of the possible samples into displayed points. Scopes with slower update rates take an even smaller percentage of the possible samples. Digital scopes don't always operate at their maximum sample rate, however, particularly on the slower sweep-speed settings, so the efficiency is often higher.

On most scopes, the dead-time/display-rate performance changes with time/division setting. Using the HP 54600B as an example, on slow timebase settings, the time/division that the user selects limits the display-update rate. For example, at the 10-msec/div setting, acquiring the samples takes  $10 \text{ div} \times 10 \text{ msec} = 100 \text{ msec}$ . The HP 54600B processes these samples to the display essentially in real time, so the duty cycle approaches 100%.

On faster time/division settings, the scope dead time becomes significant. For example, on the 100- $\mu\text{sec}$ /division setting, the time to acquire the samples is 1 msec. The dead time is approximately 1.3 msec, so the duty cycle is  $1 \text{ msec} / 2.3 \text{ msec} = 43.5\%$  (Ref 2). Again, this scope has a fast display update rate. Many scopes have much lower duty cycles.

How fast does the sample rate need to be? Even though the Sampling Theorem (Ref 3) states that the sample rate should be greater than twice the scope bandwidth, practical considerations can make you want an even higher sample rate. On the other hand, various repetitive sampling techniques can enable a scope to acquire a waveform, despite using a sample rate lower than the Nyquist rate (a sample rate equal to twice the highest frequency component present in the signal). These techniques work only on repetitive waveforms, however. In an ideal sense, you'd like to make the sample rate so high that you can forget about it, but doing so is expensive (Ref 4).

### Classes of signals

To get a handle on how sample rate and dead time affect scope measurements, divide all the waveforms in the world into three main categories (Ref 5):

- **Single-shot waveforms:** Transient events that occur only once,
- **Repetitive waveforms:** Simple waveforms that repeat over and over without any variation in waveshape, and
- **Varying repetitive waveforms:** Waveforms that basically repeat but have some variation in their waveshape, including very infrequent events.

Some waveforms might not fit easily and cleanly into one of these categories, but these waveform categories help you understand how sample rate and dead time affect the quality of a measurement.

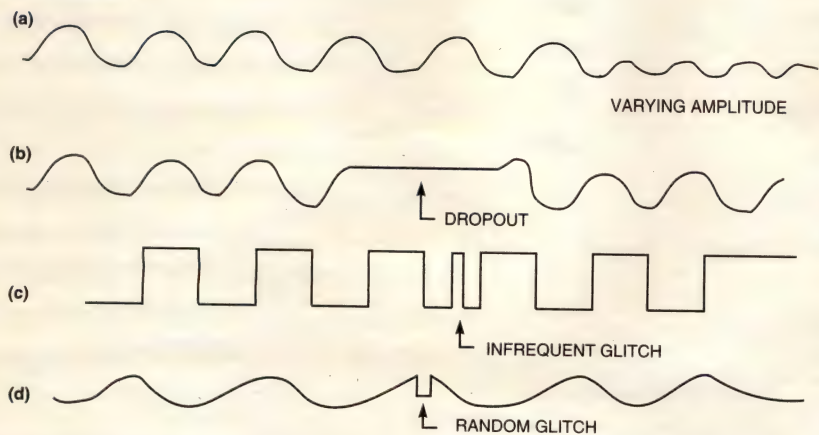
Understanding single-shot waveforms is simple. Single-shot waveforms occur only once, so you get only one chance to measure them. Alternatively, they occur so infrequently that it seems as though you get only one chance to measure them. Either way, the scope must have sufficient sample rate to capture the event and store it in memory. Again, you could argue about how high the sample rate needs to be to capture the signal faithfully, but a sample rate above the Nyquist frequency is a minimum requirement.

If you have only one chance to capture a signal, the scope needs to know when the signal occurs, which leads to the issue of triggering. Triggering is a key feature in all scope measurements, but it deserves special mention here, because if you can't trigger on a single-shot event, you will never see the event. If the event is something simple, such as a single pulse, edge triggering should be sufficient to capture the event.

If the event is more complex, you need a more sophisticated triggering capability. Suppose the single-shot event is a single narrow pulse in a stream of wider pulses. This is a single-shot event, but it's in a signal that hides it from an edge trigger. A trigger feature such as glitch trigger or time-qualified pattern trigger could identify the one narrow pulse in the signal and trigger on it. Most high-sample-rate scopes for single-shot capture include an advanced triggering system. Although triggering is an important issue for single-shot signals, dead time is not. Because the event occurs only once, there is no need to quickly acquire a second event.

Repetitive waveforms are also easy to understand. The classic function-generator waveforms—sine, square, and triangular waves—all fall into the repetitive category. Most scopes display these waveforms well because the waveforms don't vary and triggering on them is usually easy. Sample rate is not a big issue for these measurements;

FIGURE 2



**Repetitive waveforms that don't repeat exactly are varying repetitive waveforms. They present challenges for most DSOs.**



another cycle of the waveform will come along soon enough, so the scope can use repetitive sampling. Repetitive signals are not necessarily simple, though; complex signals, such as composite video, can be repetitive.

### If the scope doesn't trigger...

To effectively view repetitive signals, you need to trigger on them; otherwise, they are unstable and wander across the display. Simple signals require only edge triggering, but others, such as composite video, can require other trigger modes.

Dead time is not a big issue for truly repetitive signals. The scope need not be in any great hurry to acquire the next cycle; a cycle just like it will be along when the scope is ready. Don't neglect dead time, however, because the scope's responsiveness depends on a quick acquisition system. Scope users expect a signal to appear instantly when they move a probe from point to point in a circuit. Also, the scope should respond instantly to changes in its front-panel settings. Scopes with long dead time (sluggish acquisition systems) tend to respond sluggishly to changes in control settings.

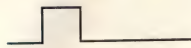
Varying-repetitive waveforms are more difficult to understand than the previous two categories but represent an important and common class of waveforms that are often difficult to measure. Think of these waveforms as basically repetitive with some variation in the waveshape. For example, a sine wave that varies in amplitude as a function of time is basically repetitive but varies from cycle to cycle. This variation might be very slow, producing a scope display that shows a sine wave gradually changing in size. Alternatively, the variation could be very fast, occurring instantly on only one cycle of a waveform. The slowly varying case is easy to view with almost any scope, but the quickly varying signal presents a greater challenge. A scope with a short dead time and a high display rate is more likely to show the single short cycle, assuming that the scope triggers on the normal cycles of the sine wave. If the scope can trigger on the reduced-amplitude cycle, the measurement problem degenerates to the single-shot case.

Fig 2 shows some representative examples of varying repetitive waveforms. Often, these signals are the unexpected ones that make an engineer's or technician's job difficult. These are the hardware bugs that are unavoidable even though you never intentionally design them into a circuit.

Sample rate is a confusing issue for varying-repetitive waveforms. The repetitive nature of the waveform means that you can use repetitive sampling to acquire the waveform. But what about waveform variations? How well will repetitive sampling follow these variations? Using the sine-wave example, if the amplitude variation is slow, repetitive sampling with sufficiently small dead time easily keeps up

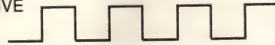
FIGURE 3

SINGLE SHOT



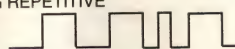
SAMPLE RATE MUST BE ABOVE NYQUIST RATE. SCOPE MUST BE ABLE TO TRIGGER ON EVENT. DEAD TIME IS NOT AN ISSUE.

REPETITIVE



SAMPLE RATE AND DEAD TIME ARE NOT USUALLY CRITICAL.

VARYING REPETITIVE



SHORT DEAD TIME AND HIGH DISPLAY RATE ARE IMPORTANT FOR VIEWING VARIATIONS IN THE WAVEFORM.

**You can divide waveforms into three major classes. Accurately measuring each class requires somewhat different scope characteristics.**

with the waveform variations. The case of one reduced-amplitude cycle is less clear; you can't be sure how many times you will sample a particular cycle unless you look carefully at the sample rate, the period of the sine wave, and how often the reduced-amplitude cycle occurs. Fig 3 summarizes the three waveform categories and their characteristics.

### A few examples

A look at some practical measurement examples will help you to apply these principles.

**Varying-width pulse:** This waveform is a repeating pulse whose width normally varies from 30 to 50 nsec and occasionally jumps to 80 nsec. This situation is common in digital systems in which the mostly nominal clock cycles are accompanied by an occasional worst-case cycle that is longer than the rest.

If you use a scope with a long dead time to measure the signal, the chances of capturing the variation in the pulse are very small. You can simulate this case by setting a large trigger hold-off on an HP 54600B scope to increase the normally small dead time (Fig 4a). In Fig 4a, the pulse appears to have little or no variation. Fig 4b shows the measured waveform with the scope operating normally, showing the pulse width varying from 30 to 50 nsec. You can't easily see the longer 80-nsec cycle, but occasional samples may fall on such a pulse. The scope operates on a timebase range that uses repetitive sampling. Even though the pulse variation is infrequent, enough of the repetitive samples fall on the wide pulse to create a useful display.

DSOs normally discard older sample points as new ones become available. This technique makes perfect sense in most situations, but when dealing with infrequent events, you might do better to keep all the sample points you can. Most digital scopes provide an infinite-persistence mode that accumulates all samples on the display. (The HP 54600-series scopes' Autostore mode has the added benefit of showing the old samples in half-bright intensity and the most recent samples in full-bright intensity.) Regardless of the dead time, using the infinite-persistence mode helps uncov-



## MEASURING WAVEFORM VARIATIONS WITH DSOs

er infrequent variations in the waveform. Fig 4c shows the varying pulse measured with the Autostore display mode. The extremes of the pulse width are now visible, including the 80-nsec-wide cycle.

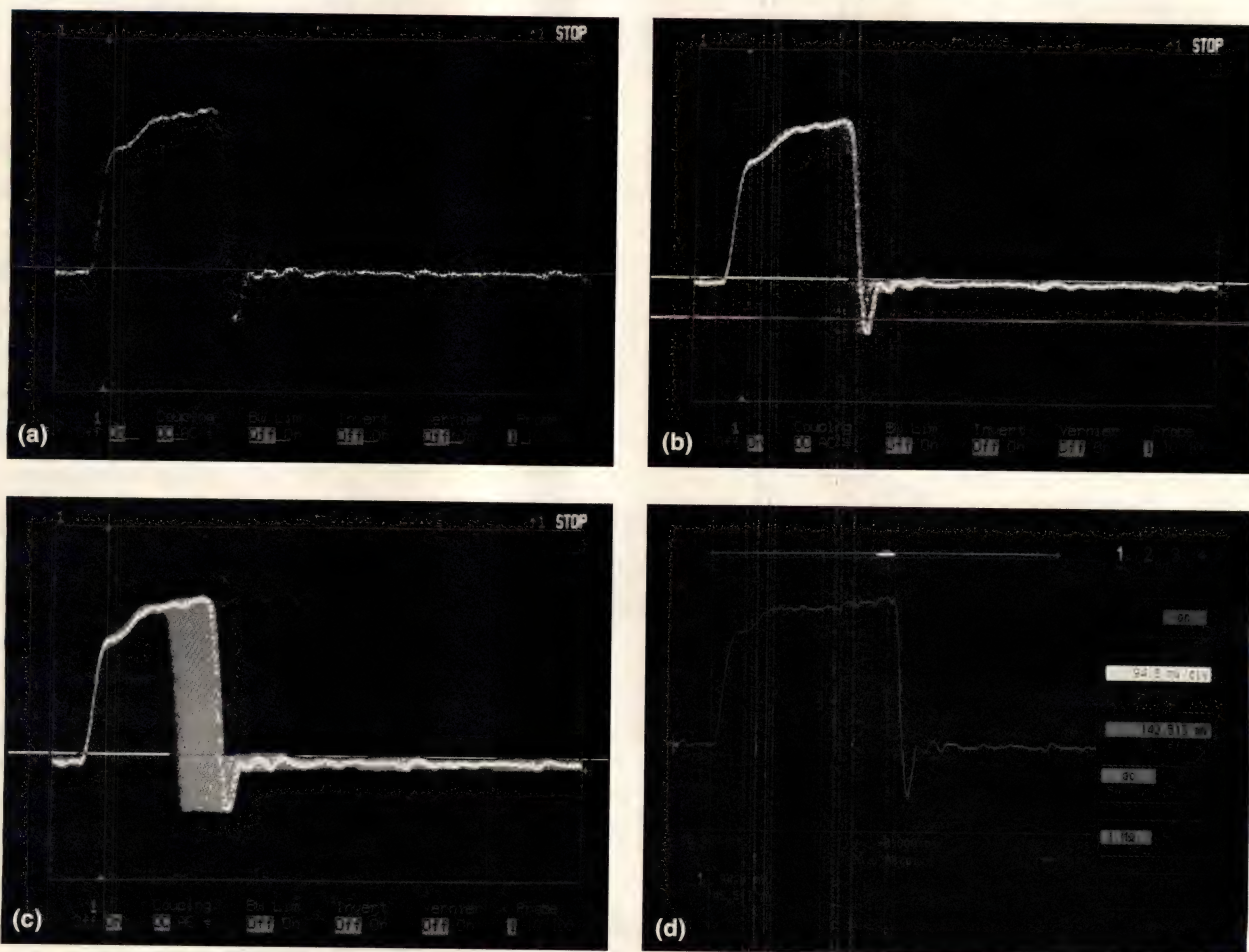
Another way to capture the wider pulse is to use a scope that can trigger on the event. For example, the HP 54542A provides a glitch-trigger feature that can trigger directly on the wider pulse. With the glitch trigger set to trigger on pulses  $\geq 60$  nsec wide, you can easily capture and display the wide pulse (Fig 4d). Using this triggering capability along with a sample rate high enough to capture the event in one acquisition generally provides the best measurement of the waveform. To use this capability, you must know what to trigger on, however.

**Sine wave with dropout:** This signal is a basic sine wave that occasionally drops out, leaving a 0V baseline in place of a sine-wave cycle.

A scope with a long dead time tends to miss the flat baseline (Fig 5a). You might conclude that the sine wave is continuous and that the signal source is operating correctly when, in reality, the signal drops out occasionally. Shorter dead time causes the waveform imperfection to easily appear (Fig 5b). Again, the scope is operating at a timebase setting that uses repetitive sampling, showing that repetitive sampling is useful for identifying waveform irregularities.

Again, if you know what to trigger on, you may be able to use the information to trigger directly on the event. Many scopes with advanced logic triggering can directly trigger on

**FIGURE 4**



If you use a scope with a long dead time (a), you might think that you were looking at a very stable waveform. An HP 54600B with trigger hold-off simulates the long dead time. A scope with a shorter dead time, in this case, an HP 54600B without trigger hold-off (b), shows that the pulse width varies considerably. Turning on the Autostore infinite-persistence feature (c) makes the variations in the pulse width much more visible. With its glitch-trigger capabilities and high sample rate, the HP 54520A can capture a picture of the pulse train's widest pulse (d), even if the wide pulse occurs only once.



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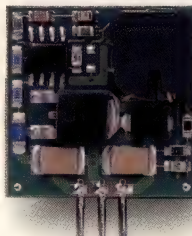
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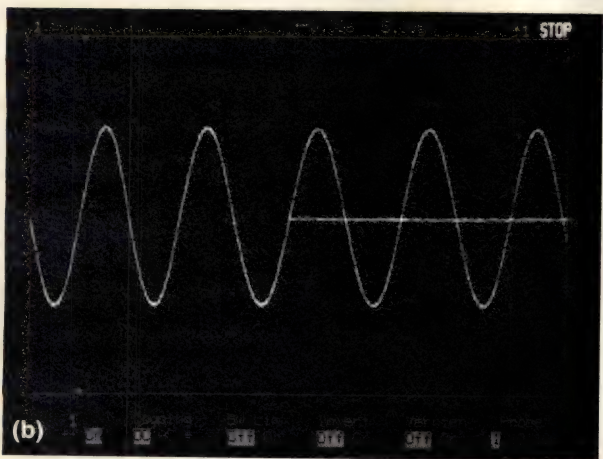
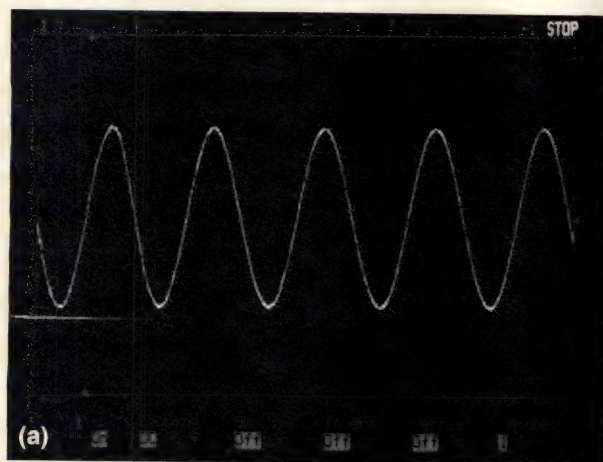
## MEASURING WAVEFORM VARIATIONS WITH DSOs

the waveform. On the other hand, even the most advanced triggering system can't capture some signals. For example, a small dip in the amplitude of a sine wave would be difficult to trigger on. Although scope manufacturers keep creating more powerful triggering systems, there will always be cases in which the scope cannot trigger on the waveform variation.

### Triggering vs display rate

Triggering plays a role in viewing infrequent events. If you can trigger on an event of interest, you essentially reduce the problem to the single-shot case and eliminate the dead-time issue. How does this stratagem fit into everyday scope use?

FIGURE 5



Although you can't tell if you use a scope with a long dead time (a), this sine wave is not continuous. Occasionally, the signal source drops out—it produces only a baseline for an entire cycle. An HP 54600B with trigger hold-off simulates the long dead time. When you use a low-dead-time scope (b), the dropout in same sine wave appears clearly. The HP 54600B also acquired this waveform, but without trigger hold-off.

Triggering is often the ultimate solution to viewing a tough problem, provided that you can describe and trigger on the problem. In troubleshooting, you often don't know what the problem is; otherwise, you'd have fixed it by now. In such cases, a high-update-rate scope that doesn't miss much between acquisitions may be the best choice.

In summary,

- For single-shot measurements, there is no substitute for a fast sample rate.
- For repetitive measurements, sample rate is less of an issue; most scopes display repetitive signals quite well.
- For varying repetitive signals, scope dead time and display-update rate become critical. During its dead time, the scope cannot see variations in the signal.
- Triggering can be a powerful way to measure infrequent events but requires some knowledge of the event on which you want the scope to trigger.

How do you determine the dead time of a digitizing oscilloscope? Well, it depends. Some scopes specify their displays update rate or dead time, but most don't. In general, a scope manufacturer that designed a scope for a fast display update rate will specify the rate. If there is no spec, you must determine the rate through experimentation.

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## Author's biography

Robert Witte has worked at Hewlett-Packard for 16 years. Witte is an R&D project manager who heads a team of engineers designing digital oscilloscopes and related instruments at HP's Colorado Springs, CO, facility. A senior member of the IEEE, he holds a BSEE from Purdue University, West Lafayette, IN, and an MSEE from Colorado State University, Fort Collins, CO. He lists his hobbies as amateur radio and backpacking.

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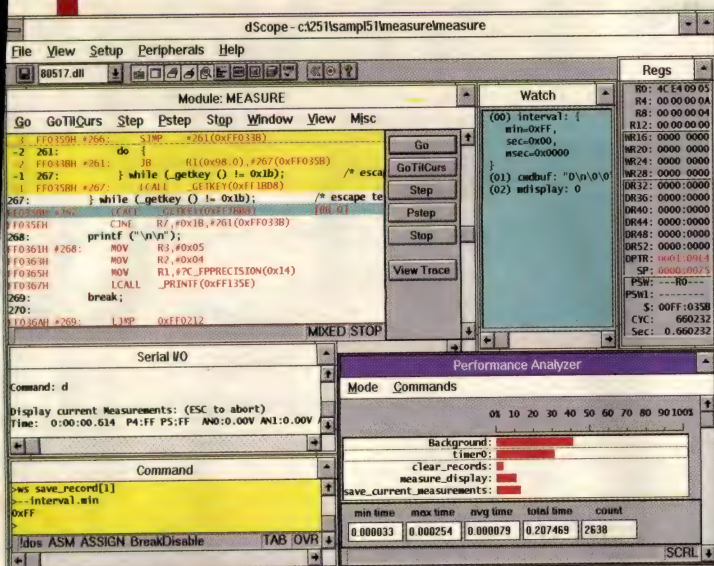
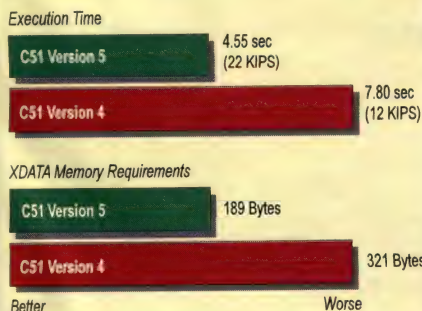
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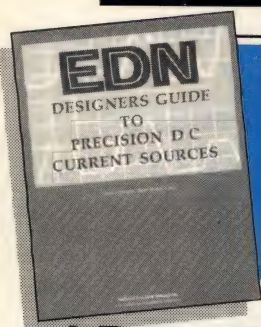


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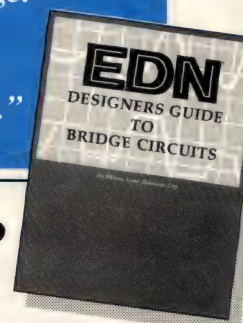


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# Fixed or floating? a pointed question in DSPs

*JIM LARIMER AND DANIEL CHEN, TEXAS INSTRUMENTS*

The most fundamental difference between fixed- and floating-point DSPs is the numeric format. The hardware of fixed-point DSPs uses integer arithmetic. Floating-point DSPs perform integer, or real, arithmetic. Normally, floating-point DSP formats are 32 data bits wide, in which 24 bits form the mantissa and 8 bits make up the exponent. For example, the chip would store the decimal value 194 (exponent) and a 10314575 (mantissa) as 1100 0010 1001 1101 0110 0011 0100 1111.

In an application, the mantissa defines precision, and the exponent designates dynamic range. For example, in a missile-tracking system, each unit in the mantissa might represent an arc-second, and the exponent might indicate how many arc-degrees the entire tracking field included (how wide the field was overall).

Because fixed-point DSPs perform integer arithmetic, no exponent is included in the numeric format. Normally, fixed-point DSPs are either 16 or 24 data bits wide. A 24-bit fixed-point DSP offers the same precision as the 24-bit mantissa of a floating-point DSP. However, the fixed-point DSP does not offer the greater dynamic range of the floating-point DSP's exponent. Thus, with a fixed-point DSP, the missile-tracking system would be limited to a specific number of arc-seconds.

Consequently, the end use often determines the type of device a designer should choose. Factors that you should consider include power consumption, performance, programmability, packaging, and price.

## **Architecture determines the application**

The numeric format makes floating-point devices ideal for more complex operations in high-performance applications. However, the architectural differences give fixed-point devices a leading edge for high-volume, low-power applications.

**Designers considering DSP applications must first decide whether to commit their designs to fixed- or floating-point DSPs. The answer may seem to be a trade-off between cost and performance. However, designers must carefully consider a variety of factors before choosing a DSP.**

Because of its 32-bit instruction-word width, the floating-point DSP's instructions can be more powerful than the 16-bit instruction words of fixed-point DSPs. Although the MIPS ratings are higher for fixed-point DSPs, the 32-bit floating-point instructions support additional parallel operations.

Floating-point DSPs currently have a larger address width of 24 bits, compared with 14 or 16 bits for fixed-point DSPs. Fixed-point DSPs, which are used primarily in embedded applications, have a smaller address reach to reduce the number of external pins the application requires. Floating-point DSPs, which are optimized for system-level processing, are less sensitive to cost and require a larger address reach. Consequently, floating-point DSPs direct correspondingly larger areas of memory for greater data and program storage.

However, the floating-point DSP's greater word and address widths can add up to greater power consumption. Typically, the 16-bit fixed-point device's bus size allows it to fit into a smaller package and consume less power. You can operate the fixed-point device at faster speeds because of its relatively simple architecture and fewer speed paths.

Newer fixed-point DSPs provide application-specific instructions and on-chip power management for portable and mobile communications applications. Many designers are fine-tuning upcoming industry standards for 16-bit fixed-point implementations because of this implementation's prevalence in the mobile market. In addition, on-chip memories are fine-tuned to meet the needs of certain applications, such as digital cellular phones. The addition or elimination of certain peripherals, such as a host port, a UART, or a buffered serial port, is an option for the new fixed-point DSPs as well.

Traditionally, software development has been slower with fixed-point devices. However, breakthroughs in fixed-point design are improving the development-cycle time. For



## DSPs

example, in a fixed-point implementation of a voice compression specification for the US digital cellular standard IS-54B, improved compiler support and a more orthogonal instruction set have greatly reduced development-cycle time for cellular phones.

Designers must weigh performance, power, and size with other important factors—device and system costs. Cost, of course, is a significant factor for many applications. In general, fixed-point DSPs tend to cost less. However, the application determines cost efficiency.

**Table 1** highlights the differences between fixed- and floating-point DSPs. In general, fixed-point DSPs are lower cost devices. Designers, therefore, tend to use these devices in high-volume embedded applications. In contrast, designers use floating-point DSPs for system-level control in which performance, not cost, is the main concern.

Fixed-point DSPs are more peripheral-rich and include such functions as host ports, asynchronous and synchronous serial ports, buffered serial ports, and capture/compare. In addition, fixed-point DSPs with on-chip peripherals can rival floating-point processors in price, but fixed-point DSPs also help to save space and cost for other components. As a result, even the high-priced fixed-point devices tend to save on systemwide costs. With a greater peripheral and memory, fixed-point DSPs allow designers to match system requirements exactly.

Although the greater dynamic range and programming ease of floating-point operation come at a cost, some applications must have the higher floating-point format. The high-level language combined with the large address reach offered by the floating-point device make it ideal for applications such as workstations.

**Table 2** lists the most important factors a designer must

**TABLE 1—IMPORTANT FEATURES OF FIXED- AND FLOATING-POINT DSPs**

Architecture	Fixed-point Integer arithmetic (real in software) 16-, 24-bit data width 14-, 16-bit address width Accumulator-based	Floating-point Integer and real arithmetic in hardware 32-bit data width 24-, 32-bit address width Register-based
Application	Embedded processor More on-chip peripheral options Lower systemwide device cost	System-level processor Greater parallelism Faster software development

consider when deciding between a fixed- or floating-point DSP. The top of the table rates the DSPs from 0 (least favorable) to 5 (most favorable) for each of the design factors. The bottom of the table indicates typical applications in which these design factors are critical.

Because power consumption, cost, and size are benefits of fixed-point DSPs, these devices are obvious choices for cellular phones, modems, and hard-disk drives. However, for graphics and imaging, floating-point calculations and performance are indispensable, so these applications use floating-point DSPs.

Voice mail needs the low cost of a fixed-point DSP and the rapid development of a floating-point DSP. Voice-mail system developers may choose to use floating-point DSPs for low-volume, high-profit systems that handle 100 or more phone lines. The designers can redevelop the system using fixed-point DSPs for high-volume, low-cost systems that handle only a few phone lines.

### Consider all features

Certain features of product selection and support may also affect your DSP choice. The additional development time of fixed-point operation may be cost-effective, depending on

(continued on pg 119)

**TABLE 2—DESIGN FACTORS TO CONSIDER**

	Cost	Power consumption	Performance	Package size	Development time	Floating-point capability
<b>DSP type</b>						
Fixed-point	4	5	3	4	3	0
Floating-point	1	2	4	1	4	5
<b>Application</b>						
Cellular phone	X	X	X	X		
Add-in modem	X		X			
PCMCIA modem	X	X	X	X		
Hard-disk drive	X	X		X		
Voice mail	X		X		X	
Graphics			X			X



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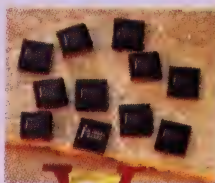
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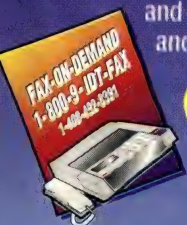
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## DSPs

these features. Before choosing a DSP, you should investigate:

- The availability of software tools and development platforms;
- Whether a DSP architecture is available for the application. For instance, DSPs designed for audio/video decompression can be cost-effective for some consumer systems, although off-the-shelf DSPs may not be;
- The availability of off-the-shelf software modules for the application;
- Your ability to customize the DSP with added memory or logic for the application;
- The dynamic range that the application requires; and
- The packaging and parallelism requirements.

The choice of a fixed- or floating-point DSP for an application may not be a simple trade-off between cost and performance. The floating-point processor's dynamic range and ease of development, the fixed-point processor's simple architecture and on-chip peripherals, and your product selection and support affect your choice. A designer needs to explore all options to choose the right DSP.

EDN

## Authors' biographies



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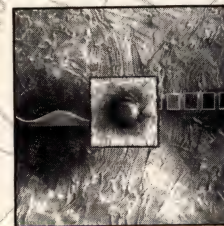
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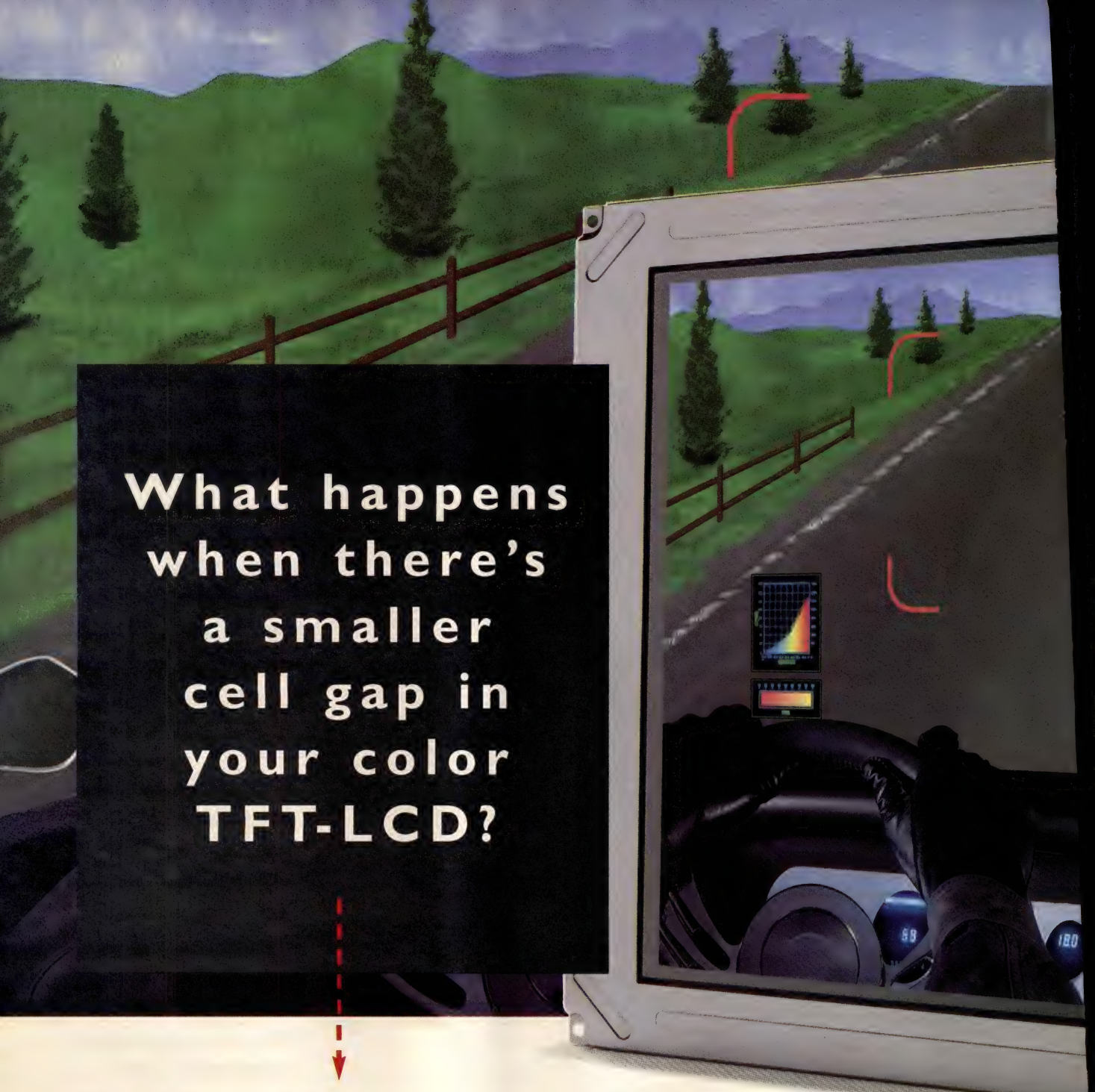
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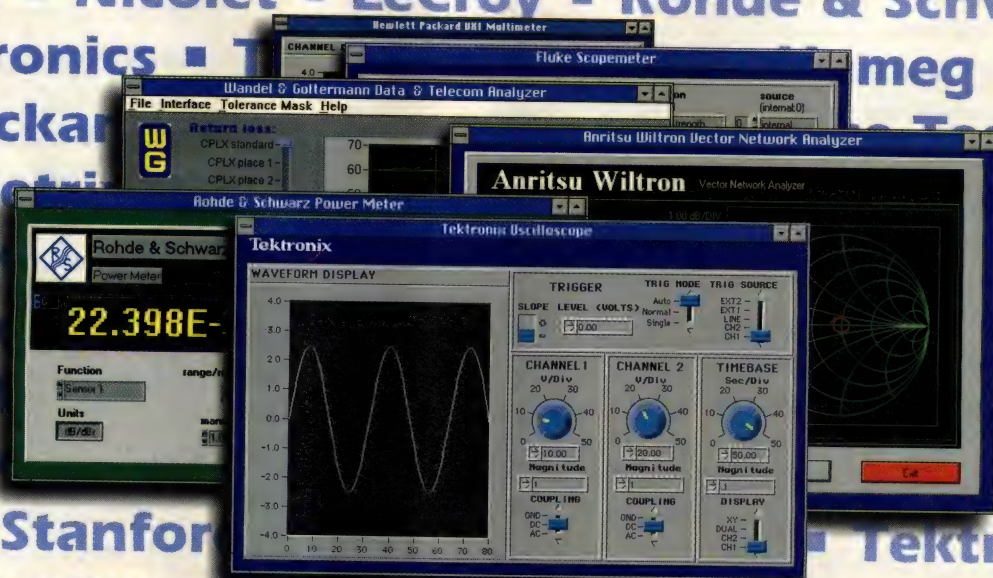
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# Improved circuit-analysis techniques require minimum algebra

VATCHÉ VORPÉRIAN, JET PROPULSION LABORATORY,  
CALIFORNIA INSTITUTE OF TECHNOLOGY

Systematic nodal or loop analysis is the universally adopted formal method of teaching network theory at the undergraduate level. Although the matrix algebra of formal network analysis is ideal for numerical computation on a computer, it fails when you're looking for analytical answers or trying to acquire more insight into a circuit's operation.

Consequently, for most analog-design engineers, the only route to a better understanding of circuits (with a goal of designing improved ones) is the slow process of cut and try.

When designing circuits, most analog engineers rely largely on experience and trial-and-error methods, eschewing much of the matrix algebra they learned in college. Using the Extra Element Theorem, however, is a helpful analytical technique that can yield insight into network design.

As you follow this route, you'll find yourself either breadboarding circuits or simulating them using CAD tools—but not using the analytical methods you learned in school.

Professor RD Middlebrook, a consultant and educator at California Institute of Technology (Caltech), recognized this problem. He developed efficient analytical

methods that derive faster and better analytical answers and avoid the horrors of runaway algebra (Refs 1, 2, and 3). One analytical method, which is called the Extra Element Theorem (EET), cuts through the algebra (see box, "The EET specialized to an impedance function"). For a general discussion and derivation of the EET, see Ref 2.

The circuit in Fig 1 is borrowed from a well-known textbook by LO Chua and Pen-Min Lin (Ref 4). In Fig 1, input resistance is to be determined as a function of the transconductance ( $g_m$ ) using the parameter-extraction method. Because the parameter-extraction method requires a considerable amount of matrix manipulation, which would become prohibitively complex if all elements were in symbolic form, Chua and Lin assigned numerical values to the resistors:  $R_1=1\Omega$ ,  $R_2=0.2\Omega$ ,  $R_3=0.5\Omega$ ,  $R_4=10\Omega$ , and  $R_b=0.1\Omega$ . The resulting input resistance is

$$R_{in} = \frac{96.3 + 5.1g_m}{137.7 + 10.5g_m} \quad (1a)$$

which can be rewritten by making the leading term in the numerator and the denominator unity:

$$R_{in} = 0.7 \frac{1 + g_m 5.3 \times 10^{-2}}{1 + g_m 7.6 \times 10^{-2}} \quad (1b)$$

Note from Eq 1b that if  $g_m$  is 0, then  $R_{in}=0.7\Omega$ .

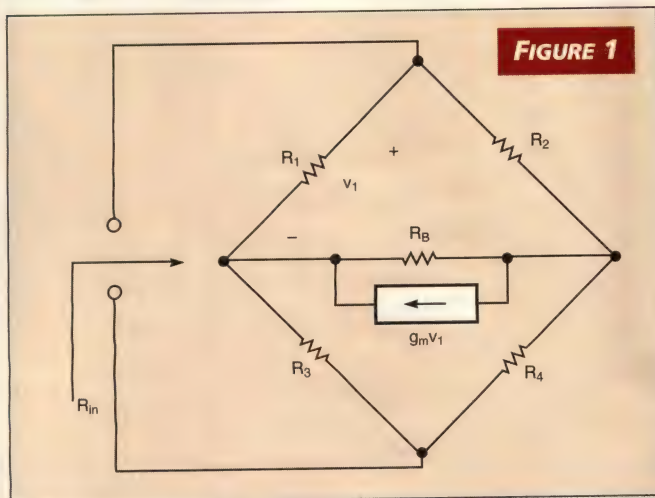


FIGURE 1

In this example, input resistance is to be determined as a function of the transconductance  $g_m$ . Assigning numerical values to the resistors ( $R_1=1\Omega$ ,  $R_2=0.2\Omega$ ,  $R_3=0.5\Omega$ ,  $R_4=10\Omega$ , and  $R_b=0.1\Omega$ ) simplifies the calculations but fails to provide a symbolic solution.



## CIRCUIT ANALYSIS

The result of Eq 1b illustrates the shortcomings of tedious traditional analysis techniques. Matrix manipulation yields

results for specific numerical values of network elements but fails to provide symbolic expressions for circuit parameters

### THE EET SPECIALIZED TO AN IMPEDANCE FUNCTION

In general, the Extra Element Theorem (EET) can be applied to the determination of any kind of transfer function, such as voltage, current, or loop gain, and can be extended to two or more extra elements. The following derivation is for an impedance function.

In Fig A, part a shows a circuit for which  $Z_{in}$  is to be determined. Let  $Z_1$  be an impedance element connected across port 1 such that if  $Z_1$  were taken out of the circuit, the determination of  $Z_{in}$  would be greatly simplified (as in the example of the bridge circuit in the main text). In essence, the EET is a

"tool" that helps you do just that. Here's how it works:

- Take  $Z_1$  out and determine  $Z_{in}$  as  $Z_1$  goes to infinity (see part b).
- With the input port shorted, look into port 1, across which  $Z_1$  was connected, and determine  $Z_s^{(1)}$  (part c).
- With the input port open, look into port 1, across which  $Z_1$  was connected, and determine  $Z_o^{(1)}$  (part d).
- To obtain  $Z_{in'}$ , assemble the three calculations above using the following formula, which is the EET for impedance functions:

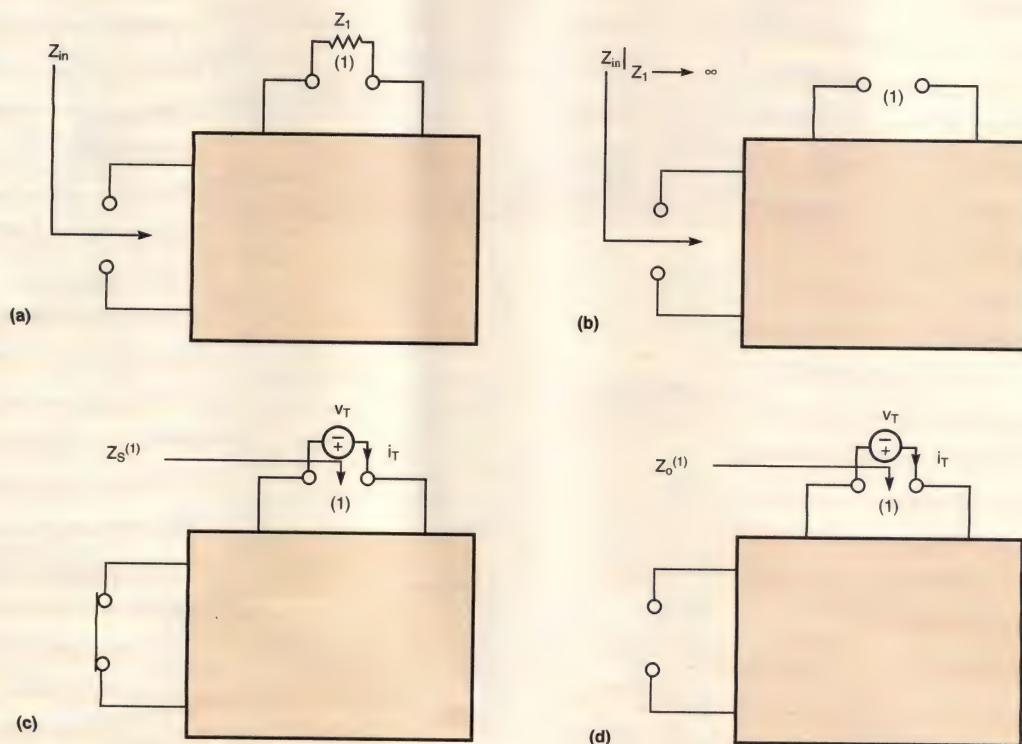
You could have made  $Z_1$  a short circuit instead of an open circuit, as in part b of the Fig A, in which case the EET

$$Z_{in} = Z_{in} |_{Z_1 \rightarrow \infty} \frac{1 + \frac{Z_s^{(1)}}{Z_1}}{1 + \frac{Z_o^{(1)}}{Z_1}}$$

would take the form

$$Z_{in} = Z_{in} |_{Z_1 \rightarrow 0} \frac{1 + \frac{Z_1}{Z_s^{(1)}}}{1 + \frac{Z_1}{Z_o^{(1)}}}$$

FIGURE A



The EET helps to determine  $Z_{in}$  in circuits such as in (a). The process involves removing  $Z_1$  (b) and determining the impedance at port 1 with the input shorted (c) and open (d).



such as input resistance. As a result, matrix manipulation provides no insight into circuit operation. For instance, Eq

1b provides no information on how changes in  $R_1$ ,  $R_2$ ,  $R_3$ ,  $R_4$ , and  $R_b$  affect  $R_{in}$ .

You can also apply the EET when the extra element is a dependent source (any one of the four possible kinds, such as voltage-controlled voltage source, voltage-controlled current source, and so on). Part **a** shows a dependent current source controlled by  $u_2$ , which can be either a voltage or a current at some other point in the circuit. Now, apply the EET by performing the following three calculations:

- Determine  $Z_{in}$  as  $A$  goes to zero (part **b**).
- Connect an independent source ( $i_T$ ) across port 1 pointing in the opposite direction of  $i_1$  with the input port open; then, determine the inverse gain  $A_O^{(1)} = u_2/i_T$  (part **d**).
- To determine  $Z_{in}$ , assemble the above calculations using this formula:

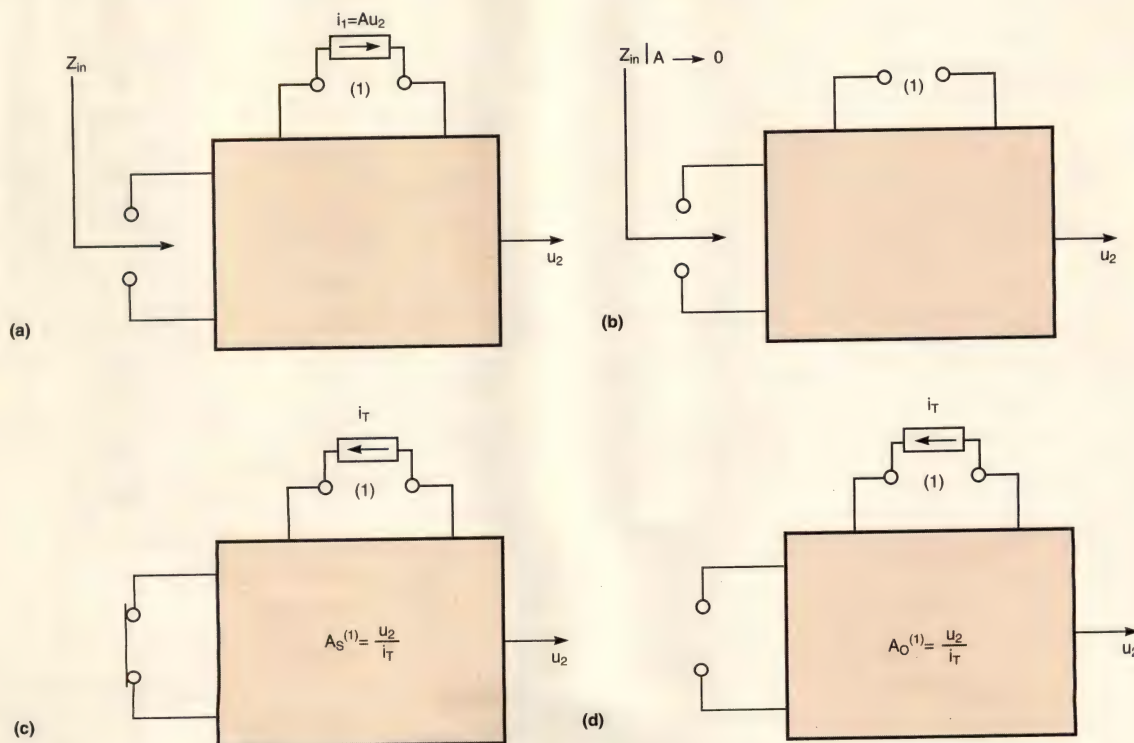
$$Z_{in} = Z_{in} |_{A \rightarrow 0} \frac{1 + AA_s^{(1)}}{1 + AA_0^{(1)}}$$

You also could have set  $A$  to infinity,

as is common for op-amp circuits, so that the EET would take the form

$$Z_{in} = Z_{in} |_{A \rightarrow \infty} \frac{1 + \frac{1}{AA_s^{(1)}}}{1 + \frac{1}{AA_0^{(1)}}}$$

**FIGURE B**



The EET proves useful when the extra element is a dependent source. Here, the extra element is a dependent current source that  $u_2$  controls; the extra element can be either a voltage or current source at some other point in the circuit.



However, you can determine such parameters in entirely symbolic form in a few simple steps using the EET twice in succession. The EET allows you to remove impedance elements and dependent sources from a circuit so you can restrict your analysis to a simpler circuit.

The two elements that most complicate the analysis of this circuit are  $g_m$  and  $R_B$ . So, first take out the dependent current source by letting  $g_m = 0$ . This step produces the circuit in Fig 2, which is an ordinary bridge circuit with input resistance  $R_{in}'$ . In trying to determine  $R_{in}'$ , note that  $R_B$  is the only element left that causes difficulty, so take it out, too. Thus, you derive the circuit in Fig 3a. Note that

$$R_{in}' = R_{in} | g_m = 0 \text{ and } R_{in}'' = R_{in}' | R_B \rightarrow \infty.$$

Looking into the input port of Fig 3a immediately shows that  $R_1$  and  $R_3$  parallel  $R_2$  and  $R_4$ , so

$$R_{in}'' = (R_1 + R_3) || (R_2 + R_4).$$

Now, two more simple calculations are required to determine  $R_{in}'$ . First, determine the resistance looking into port B, with the input port shorted as shown in Fig 3b. Note the parallel combination of  $R_1$  and  $R_3$  in series with the parallel combination of  $R_2$  and  $R_4$ , so that

$$R_s^{(B)} = R_1 || R_3 + R_2 || R_4.$$

Second, determine the resistance looking into port B with the input port open (Fig 3c). Now, if you look into port B, you see  $R_1 + R_2$  in parallel with  $R_3 + R_4$  so that

$$R_o^{(B)} = (R_1 + R_2) || (R_3 + R_4).$$

According to EET,  $R_{in}'$  is

$$R_{in}' = R_{in}'' \frac{1 + \frac{R_s^{(B)}}{R_B}}{1 + \frac{R_o^{(B)}}{R_B}}.$$

Substituting for  $R_{in}''$ ,  $R_s^{(B)}$ , and  $R_o^{(B)}$  in Eq 6, you obtain the following expression for the input resistance of a bridge circuit in which the influence of  $R_B$  on  $R_{in}$  is very clear:

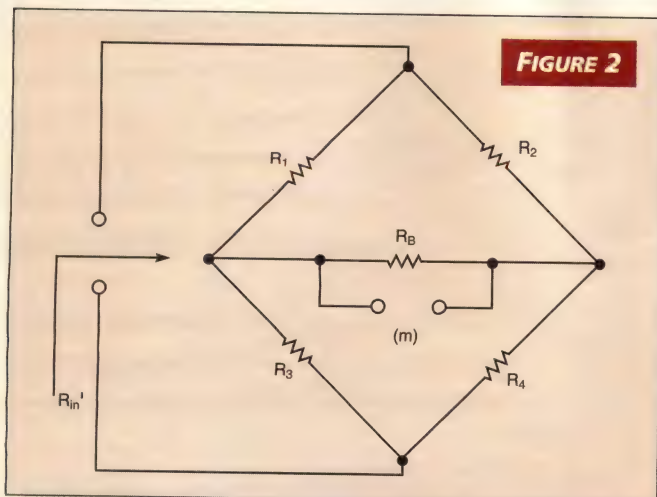


FIGURE 2

Removing the dependent source from the circuit in Fig 1 yields a simple bridge.

$$R_{in}' = (R_1 + R_3) || (R_2 + R_4) \frac{1 + \frac{R_1 || R_3 + R_2 || R_4}{R_B}}{1 + \frac{(R_1 + R_2) || (R_3 + R_4)}{R_B}}. \quad (7)$$

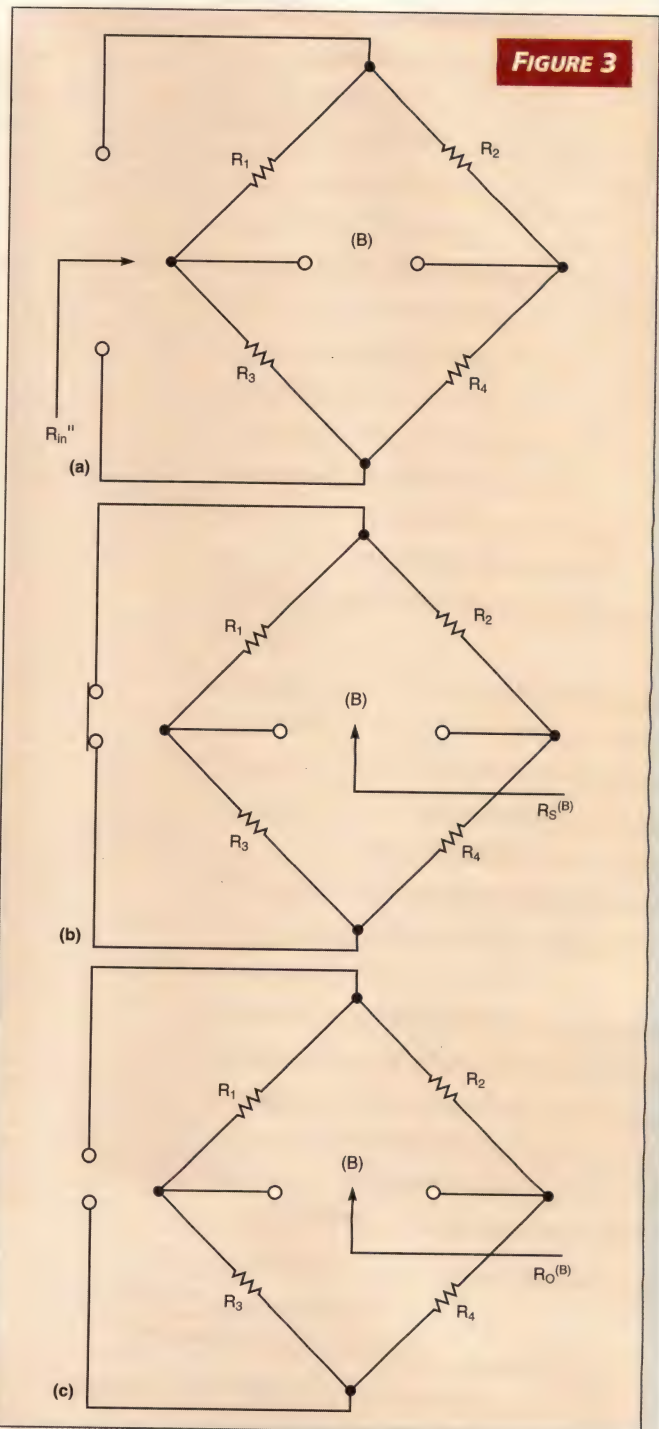


FIGURE 3

Fig 2 is the circuit in Fig 1 simplified by removal of the dependent source. In (a), removal of  $R_B$  from the circuit in Fig 2 provides additional simplification, making it easy to determine the port B input resistance with the input port shorted (b) and open (c).



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## CIRCUIT ANALYSIS

Important features of Eq 7 are that  $R_1$  through  $R_4$  appear in series and parallel combinations and that  $R_B$  appears in a ratio that can easily be compared to unity. These features allow you to simplify an expression by ignoring the smaller of two series impedances or the larger of two parallel impedances. Similarly, in the expressions of the form  $1+x/R_B$  in Eq 7, you can ignore the  $x/R_B$  term if it's small with respect to unity, or you can ignore the unity term if  $x/R_B \gg 1$ . Eq 7 is called a low-entropy expression (Ref 1) because of its highly ordered nature.

In a second application of EET, reinstate  $g_m$  by performing two additional simple calculations with the dependent current source  $g_m v_1$  replaced by an independent current source,  $i_m$ , pointing in the opposite direction (Figs 4a and 4b). First, determine the inverse gain ( $v_1/i_m$ ) (transresistance) with the input port shorted (Fig 4a). The current  $i_m$  of Fig 4a divides between  $R_B$  and the  $R_1 \parallel R_3$  and  $R_2 \parallel R_4$  combinations according to the current division formula:

$$\frac{i}{i_m} |_{(in) \rightarrow short} = \frac{R_B}{R_B + R_1 \parallel R_3 + R_2 \parallel R_4}$$

$R_1$  and  $R_3$  are in parallel because of the short on the input, so they have the same voltage drop ( $i$  times  $R_1$  in parallel with  $R_3$ ) across them. Therefore, the reverse transresistance with the input shorted is

$$A_s^{(m)} = \frac{v_1}{i_m} |_{(in) \rightarrow short} = \frac{R_B}{R_B + R_1 \parallel R_3 + R_2 \parallel R_4} R_1 \parallel R_3$$

Next, repeat the same procedure with the input port open (Fig 4b). Using the current division formula between branches  $R_1+R_2$  and  $R_B$  in parallel with  $R_3+R_4$ , you obtain

$$\frac{i}{i_m} |_{(in) \rightarrow open} = \frac{R_B \parallel (R_3 + R_4)}{R_B \parallel (R_3 + R_4) + R_1 + R_2}$$

Because the voltage across  $R_1$  is  $v_1 = iR_1$ , you get

$$A_o^{(m)} = \frac{v_1}{i_m} |_{(in) \rightarrow open} = \frac{R_B \parallel (R_3 + R_4)}{R_B \parallel (R_3 + R_4) + R_1 + R_2} R_1$$

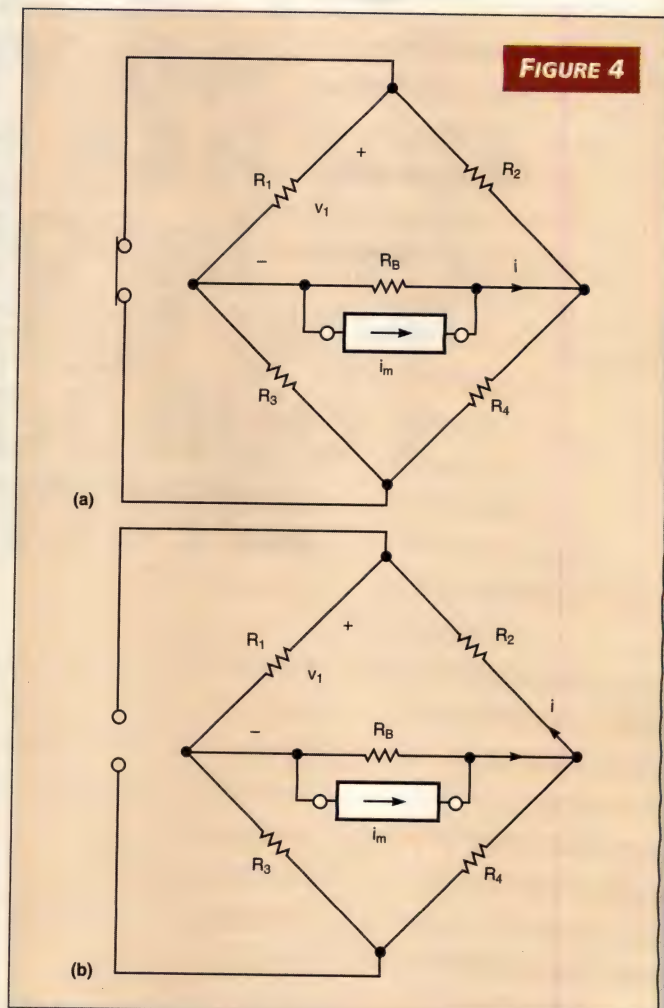
The EET now shows that  $R_{in}$  is

$$R_{in} = R_{in} |_{g_m \rightarrow 0} \frac{1 + g_m A_s^{(m)}}{1 + g_m A_o^{(m)}} = R'_{in} \frac{1 + g_m A_s^{(m)}}{1 + g_m A_o^{(m)}} \quad (10)$$

Substituting for  $R'_{in}$ ,  $A_s^{(m)}$ , and  $A_o^{(m)}$  in Eq 10 yields the desired result:

$$R_{in} = (R_1 + R_3) \parallel (R_2 + R_4) \frac{1 + \frac{R_1 \parallel R_3 + R_2 \parallel R_4}{R_B}}{1 + \frac{(R_1 + R_2) \parallel (R_3 + R_4)}{R_B}} \frac{1 + g_m R_B \frac{R_1 \parallel R_3}{R_B + R_1 \parallel R_3 + R_2 \parallel R_4}}{1 + g_m R_1 \frac{R_B \parallel (R_3 + R_4)}{R_B \parallel (R_3 + R_4) + R_1 + R_2}} \quad (11)$$

FIGURE 4



Inserting an independent current source ( $i_m$ ) is the first step toward reinstating  $g_m$ . Calculations proceed with the input shorted (a) and open (b). Note that  $i_m$  points in the opposite direction of the dependent source of Fig 1a.

The result in Eq 11 is superior to the result in Eq 1b, because it contains useful symbolic information about all the circuit elements. It is important to realize that not all symbolic expressions contain useful information unless their elements are grouped together in series and parallel combinations and ratios (Eq 11). If you were to use nodal or loop analysis, the result would have come out as a single numerator and a single denominator, each containing the sum of products of four resistances at a time. And the coefficient of  $g_m$  would contain the sum of products of five resistances at a time.

Such a high-entropy answer not only would have been prohibitively unpleasant to obtain, but also would have contained no recognizable information about the circuit's operation. Obtaining a high-entropy



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## CIRCUIT ANALYSIS

result is precisely how engineers discover that nodal- or loop-analysis techniques fail to help them understand circuit performance, even if they were to carry out the analysis and survive the algebra.

In another example of how the EET can obtain a simple low-entropy result, the bridge circuit in Fig 1 can be made reactive by replacing  $R_b$  with a capacitor  $C_b$  (Fig 5). This circuit illustrates three important points:

- A reactive circuit can be analyzed with the same ease as a resistive circuit without ever having to deal with the reactive impedance term  $(1/sC_b)$ .
- Single extraction of the parameter  $g_m$  is not useful because  $g_m$  affects the low-frequency asymptote as well as the pole and the zero of  $Z_{in}(s)$ .
- By using the EET, you can automatically determine  $Z_{in}(s)$  in factored pole-zero form.

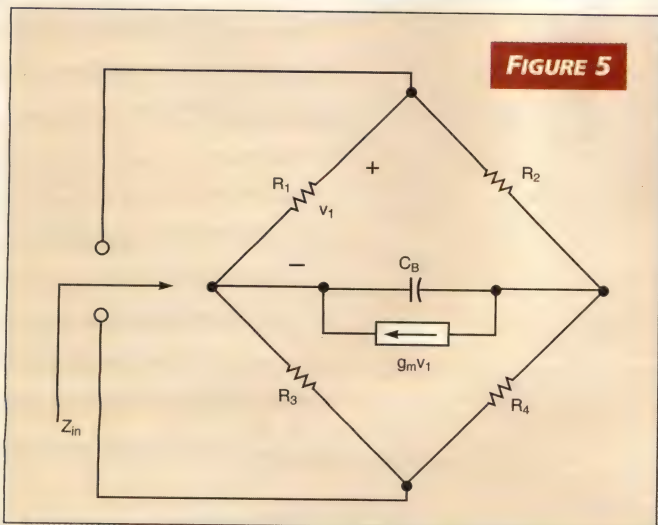
You designate the capacitive-reactance  $Z_b(s) = 1/sC_b$  as the extra element in Fig 5. Removing it from the circuit yields the circuit in Fig 6. Obtain the input impedance of this circuit from the input impedance of the original circuit in Fig 1 by letting  $R_b$  approach infinity in Eq 11. Hence,

$$R_0 \equiv Z_{in}(s)|_{Z_b \rightarrow \infty} = (R_1 + R_3) \parallel (R_2 + R_4) \frac{1 + g_m R_1 \parallel R_4}{1 + g_m \frac{R_1(R_3 + R_4)}{(R_3 + R_4) + R_1 + R_2}} \quad (12)$$

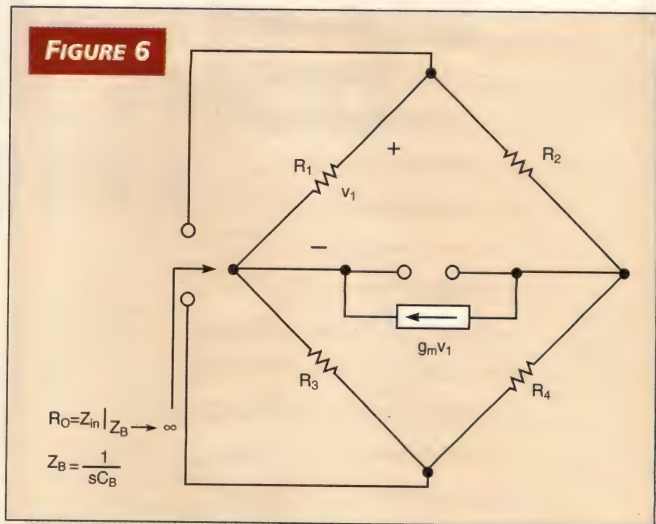
Now reinstate  $Z_b$  using the EET, which, in turn, requires that you determine port impedances  $R_s^{(B)}$  and  $R_o^{(B)}$ , shown in Figs 7a and 7b, respectively. In Fig 7a, the current  $i_T$  consists of the sum of  $g_m v_1$  and the current through the branch made up of  $R_1$  in parallel with  $R_3$  plus  $R_2$  in parallel with  $R_4$ . Therefore,

$$i_T = g_m v_1 + \frac{v_T}{R_1 \parallel R_3 + R_2 \parallel R_4}$$

In Fig 7a,  $v_1$  is related to  $v_T$  by the voltage division between  $R_1$  in parallel with  $R_3$  and  $R_2$  in parallel with  $R_4$ . Therefore,



Replacing  $R_b$  in Fig 1 with capacitor  $C_b$  demonstrates how to apply the EET to reactive circuits.



Removing the capacitive reactance from the circuit in Fig 5 yields the above circuit.

$$i_T = g_m \frac{v_T R_1 \parallel R_3}{R_1 \parallel R_3 + R_2 \parallel R_4} + \frac{v_T}{R_1 \parallel R_3 + R_2 \parallel R_4}$$

Hence, for  $R_s^{(B)} = v_T/i_T$ ,

$$R_s^{(B)} = \frac{R_1 \parallel R_3 + R_2 \parallel R_4}{1 + g_m R_1 \parallel R_3}$$

To determine  $R_o^{(B)}$ , refer to Fig 7b, where, in this case,  $i_T$  consists of the sum of  $g_m v_1$  and the currents through the branches  $R_1 + R_2$  and  $R_3 + R_4$ , so that

$$i_T = g_m v_1 + \frac{v_T}{R_1 + R_2} + \frac{v_T}{R_3 + R_4} \quad (15a)$$

Because  $v_1$  is related to  $v_T$  by the voltage division between  $R_1$  and  $R_2$ , you can rewrite Eq 15a as

$$i_T = g_m \frac{v_T R_1}{R_1 + R_2} + \frac{v_T}{R_1 + R_2} + \frac{v_T}{R_3 + R_4} \\ = v_T \frac{g_m R_1 + 1}{R_1 + R_2} + v_T \frac{1}{R_3 + R_4}$$

Hence, for  $R_o^{(B)} = v_T/i_T$ ,

$$R_o^{(B)} = (R_3 + R_4) \parallel \frac{R_1 + R_2}{1 + g_m R_1}$$

Using the EET, you obtain  $Z_{in}(s)$ :

$$Z_{in}(s) = Z_{in}(s)|_{Z_b \rightarrow \infty} \frac{1 + \frac{R_s^{(B)}}{Z_b}}{1 + \frac{R_o^{(B)}}{Z_b}} = R_0 \frac{1 + sC_b R_s^{(B)}}{1 + sC_b R_o^{(B)}}$$

which you can write in pole-zero form as

$$Z_{in}(s) = R_0 \frac{1 + s/s_z}{1 + s/s_p}$$





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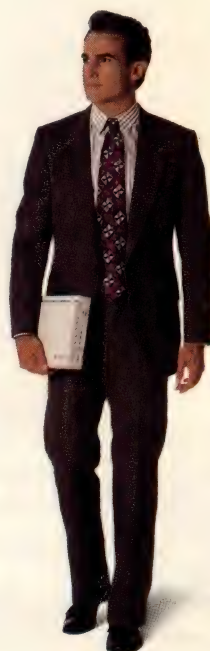
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## CIRCUIT ANALYSIS

where  $R_0$  is the low-frequency asymptote given in Eq 12, and

$$s_z = \frac{1}{C_B R_s^{(B)}} = \frac{1 + g_m R_1 \parallel R_3}{C_B (R_1 \parallel R_3 + R_2 \parallel R_4)}$$

$$s_p = \frac{1}{C_B R_0^{(B)}} = \frac{1}{C_B (R_3 + R_4) \parallel \frac{R_1 + R_2}{1 + g_m R_1}}$$

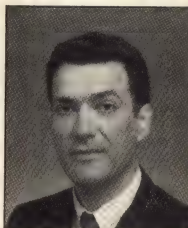
The elegance and simplicity of this derivation illustrate how, when the extra element is a reactance in an otherwise-resistive circuit, the pole and zero can each be determined independently. The EET can be applied to the process of determining any kind of transfer function, such as voltage gain, current gain, or loop gain, and can be extended to two

or more extra elements (Refs 3 and 5). Note that this work was executed by the Jet Propulsion Laboratory at Caltech, under a contract with NASA. EDN

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## Author's biography



Vatché Vorpérian holds a PhD from the California Institute of Technology (Caltech) Pasadena, CA, and is a technical-staff member of the Jet Propulsion Laboratory (JPL) at Caltech. For four years, he has assisted in developing spacecraft power supplies. Vorpérian is responsible for developing new technology and providing analytical support for the JPL's power-electronics group.

His interests include reading and attending concerts.

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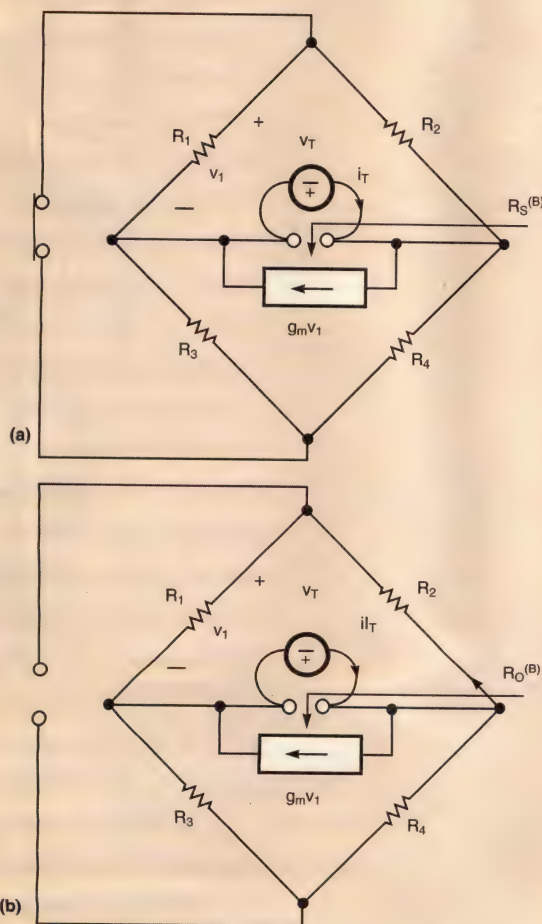
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FIGURE 7



The EET can reinstate  $Z_b$  into the circuit in Fig 6. The first step is to determine the port impedances ( $R_s^{(B)}$  and  $R_o^{(B)}$ ) for a shorted (a) and open (b) input port.





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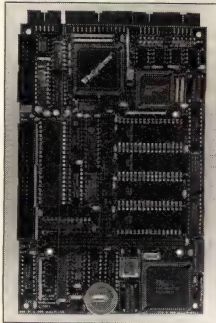
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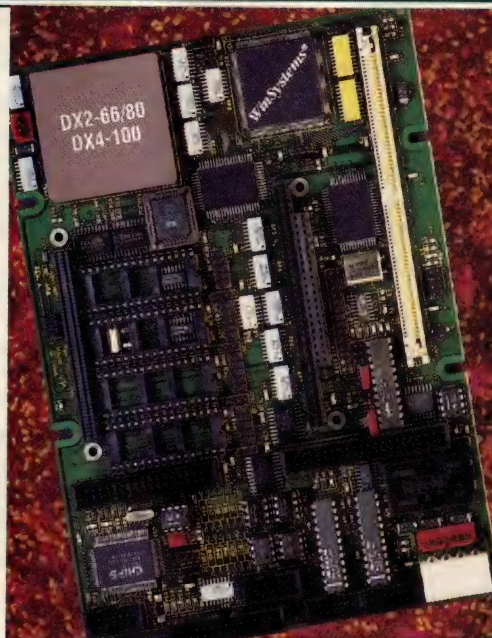
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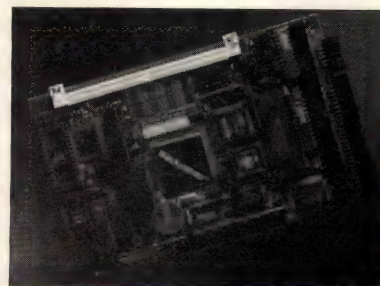


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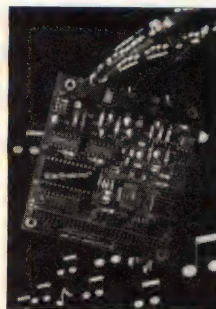
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COMMUNICATIONS  
SPECIAL ISSUE

# Isochronous LAN standard brings real-time video collaboration to the desktop

*RICH BRAND, NATIONAL SEMICONDUCTOR CORP*

One of the major goals of the computer industry is finding a way to bring multimedia collaboration capabilities to the desktop. Wide-area networks (WANs), including publicly switched services, are standardizing on integrated-services digital-network (ISDN) B and D channels for deployment of interactive multimedia communication. Thus far, such implementations have been confined to specialized video-conference rooms with direct connections to the WAN. Even though such video-conference rooms have been a driving force in establishing standards for transmission and compression of voice and video, they have lacked the flexibility and accessibility needed to empower widespread, peer-to-peer, collaborative computing.

The key obstacle to bringing such full-featured interactive multimedia capabilities to the desktop has been finding an effective way to "bridge the last 100 meters." Although most corporations can connect to the outside world via ISDN-based WANs, the majority of desktop computers in large organizations are connected by LANs, with Ethernet accounting for over 70% of today's installed base of LANs. The basic problem has been that this existing Ethernet infrastructure has not had the bandwidth or the real-time capability required to effectively support symmetrical full-duplex multimedia connections between desktops.

Ethernet's "connectionless" carrier-sense-multiple-access/collision-detection (CSMA/CD) method of controlling data-packet traffic is inherently incompatible with setting up the kind of dedicated connections needed with the public switched network. CSMA/CD is based on a concept

**IEEE-802.9a isoEthernet is the logical choice as the LAN standard of the future. It is interoperable with existing standards. It can provide seamless connectivity over public ISDN networks. And it can isolate local multimedia applications from a company's normal packet LAN/router data flow, thereby maximizing the performance of both local ISDN services and Ethernet packet traffic on the same LAN.**

that allows all nodes constant access to the network's available bandwidth, thereby ensuring a high level of interleaving between data packets and a resultant maximized use of available bandwidth. However, the reverse is also true. Because no connection between individual nodes can continuously "own" a portion of the bandwidth, all communications are subject to response-time degradation as overall network traffic increases.

The isoEthernet standard, recently adopted as IEEE-802.9a by the IEEE LAN/MAN (metropolitan-area-network) Standards Committee, can break through the WAN/LAN barrier. It brings ISDN channels directly to individual desktops over existing Ethernet type 3 unshielded-twisted-pair (UTP) networks, with no adverse impact on the Ethernet data-packet traffic being carried over those same physical networks.

IEEE-802.9a isoEthernet uses the existing physical twisted-pair infrastructure of 10BaseT Ethernet but recodes the data to allow 16 Mbps of data to be transmitted instead of existing Ethernet's 10 Mbps. The additional 6 Mbits are used to switch a dedicated 96 ISDN B channels plus one D channel between the hub and the desktop. By combining Ethernet and ISDN onto a single wire without changing their behavior, isoEthernet gives existing LAN users seamless integration with WAN B channel-based multimedia services, while preserving all of the Ethernet capabilities.

Because isoEthernet preserves the existing LAN structure and integrates data from existing WAN services, the major investment required to initially implement isoEthernet is the installation of new hubs with no changes required to mission-critical data routers. However, because any standard



## LAN STANDARD

10BaseT Ethernet controller can continue to reside on the isoEthernet network, you can upgrade individual desktops on an incremental basis as the need for interactive multimedia communications expands.

Furthermore, the isoEthernet isochronous B channels are ISDN-compatible and, therefore, allow direct connection to the WAN. This close adherence to established standards lets organizations implement isoEthernet in an evolutionary fashion that preserves and extends their existing investment while greatly expanding the capabilities of the upgraded desktop machines.

### The isoEthernet architecture

Following the channel definitions contained in the IEEE-802.9 standard, isoEthernet allows for simultaneous integration of isochronous and packet-based communications by assigning the 10BaseT packet data traffic to a P channel; grouping the 96 ISDN B channels into a C channel; and using a separate 64-kbps D channel for establishment, tear-down, and maintenance of connections. In addition, a single 96-kbps M channel is reserved for conveying control and status information to the remote end of the link.

Above these four channels, the existing transport, session, application, and presentation layers remain unchanged from today's standard operation. IEEE-802.9a specifies the

isoEthernet physical layer, which resides beneath the C, P, D, and M channels and defines their connection with the physical transport medium (Fig 1).

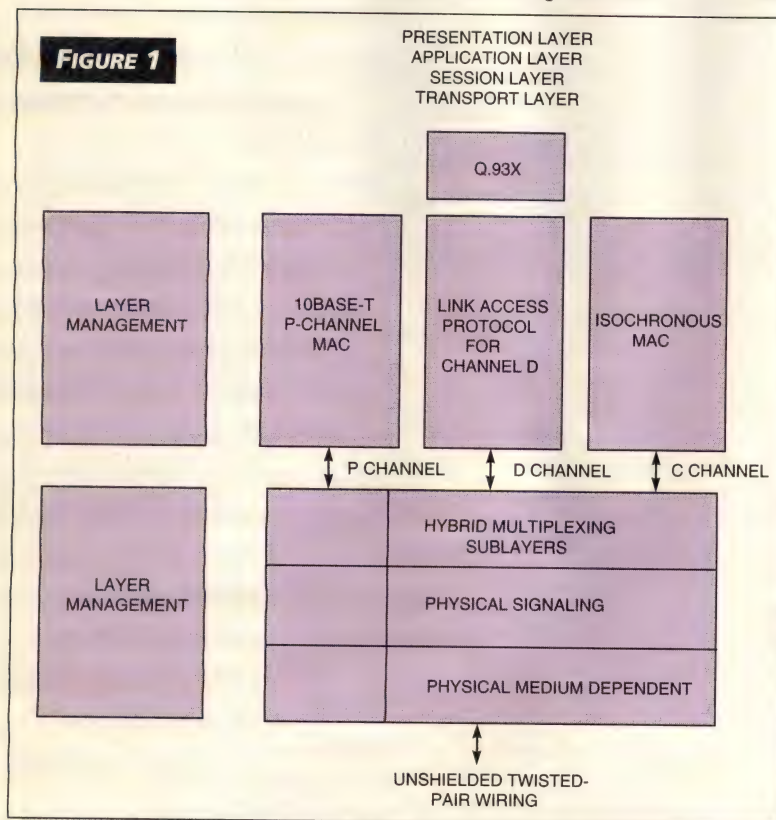
A time-division-multiplexed (TDM) information stream provisions these multiple channels on a pair of UTP wires. The information stream consists of a continuous sequence of 125- $\mu$ sec (8-kHz) TDM frames, with each frame consisting of 256 bytes of useful information. Within each frame, specific bytes are reserved to carry information corresponding to each of the multiple channels, so that every frame is guaranteed to have the bandwidth required by each of the service channels. In addition to the service-channel information, 1 byte at the start of each frame is reserved as a start-of-frame delimiter to allow the PLLs at the remote end to synchronize the incoming frame with the 8-kHz network clock.

To allow isoEthernet to be deployable in a variety of environments, the architecture makes provisions for three different operating modes:

- **Multiservice mode:** combines a 10-Mbps P channel, a 6.144-Mbps C channel (consisting of 96 ISDN B channels), a 64-kbps D channel, a 96-kbps M channel, and a 64-kbps start-of-frame delimiter
- **All-isochronous mode:** dedicates the whole service to isochronous communications with a 15.872-Mbps C channel (consisting of 248 ISDN B channels), a 64-kbps D channel, a 96-kbps M channel, and a 64-kbps start-of-frame delimiter
- **10BaseT mode:** In this mode, the isoEthernet physical layer behaves just like a 10BaseT-encoded UTP transceiver. No TDM structure is employed, and no provision for C, D, M, or start-of-frame channels is provided.

In the multiservice and all-isochronous modes of operation, the isoEthernet physical layer multiplexes the service channels into a single stream, maps the stream into a TDM frame, and performs 4B/5B symbol encoding and the line coding for serialization and NRZI (nonreturn to zero inverted). In the receive direction, it performs NRZI line decoding, 4B/5B symbol decoding, clock extraction, and the demultiplexing of service channels.

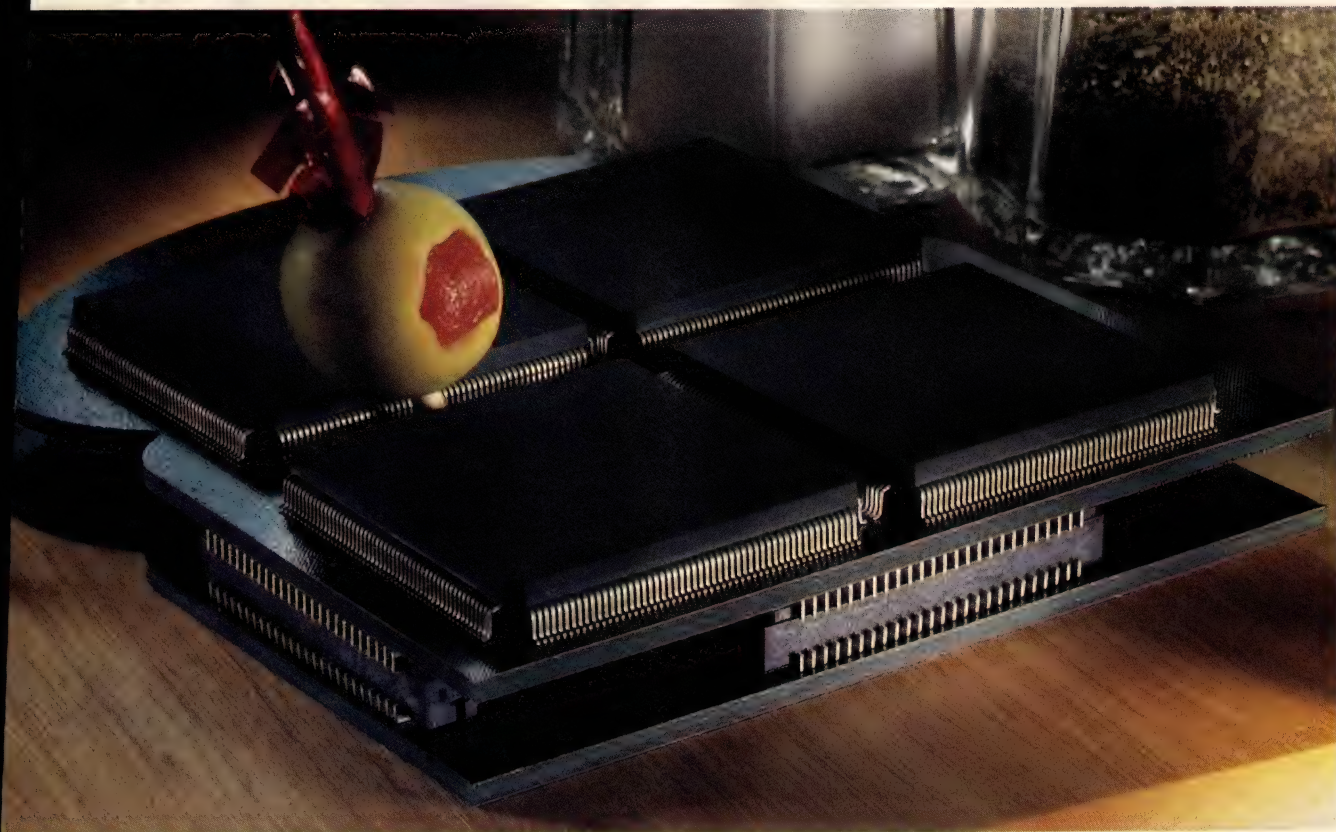
IEEE-802.9a isoEthernet codes individual octets of service-channel information using 4B/5B symbol encoding because of its inherent efficiency and ease of implementation. The encoding scheme transforms a nibble of information into a coded symbol (5-bit value) for transmission. The symbols have been specifically chosen to maintain the ac balance of the wiring and to minimize the frequency spectrum of the waveforms as they are transmitted over the wire. During normal data transmission, the dc component of the signal varies less than 10% from the nominal center. The 4B/5B, along with the NRZI line coding, provides an 80% bandwidth utilization as compared to the Manches-



The IEEE-802.9a architectural model specifies the isoEthernet physical layer, which resides beneath the C, P, D, and M channels and defines their connection with the physical transport medium.



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**CIRCLE NO. 2**

# AMP



## LAN STANDARD

ter data encoding method used in 10BaseT, which yields only a 50% bandwidth utilization (Fig 2).

This encoding scheme is the key mechanism that lets isoEthernet gain the additional 6.384 Mbps of usable bandwidth for carrying isochronous communications. Even though both 10BaseT and isoEthernet utilize a line-transmission frequency of approximately 20 MHz, isoEthernet can achieve 16.384 Mbps of usable bandwidth vs the 10 Mbps of usable bandwidth for 10BaseT.

In a manner similar to ISDN, the isoEthernet C channel can be provisioned into any multiple of 64-kbps (B-channel) bandwidth segments up to 96, depending on your application. Signaling procedures that are transported over the D channel provision these channels. These signaling procedures, as defined in the IEEE-802.9a specification, are based on the original International Telecommunication Union (ITU) Q.931 family of protocols that have already been employed in ISDN networks. This allows for easier interoperability between ISDN- and isoEthernet-based networks.

Because of IEEE-802.9a isoEthernet's compatibility with both ISDN and asynchronous-transfer-mode (ATM), organizations can easily deploy isoEthernet as a last-100-meters LAN-based link to the desktop, which can be interconnected directly to ATM backbones, ISDN WAN services, or a combination of the two. This strict adherence to standards and interoperability allows the most cost-effective evolutionary upgrading of networks as an organization's multimedia and other communications requirements grow and change. Furthermore, because both ATM and isoEthernet are ISDN-compatible, LAN/WAN/LAN connections between remotely located desktops can be easily established via isochronous links, regardless of the intervening isoEthernet, ATM, or WAN transport mechanisms.

In addition, isoEthernet's support for Microsoft's Telephony Application Programmers Interface (TAPI) allows easy porting of user applications between isoEthernet- and ISDN-connected end stations and enables such TAPI applications to interoperate. This means that designers and developers of user applications need not acquire expertise in the underlying transport technologies to create solutions that can be deployed across the different networks.

### Industry support

Successful industrywide implementation of a standard such as the IEEE-802.9a isoEthernet, which involves so many technologies, requires the resources of many types of businesses. Industry participants have formed the isochronous networking communications incAlliance; members include Apple Computer, Ascom Nexion, Dialogic, Ericsson Business Networks, IBM, ITT, Incite, Luxcom, MCI, National Semiconductor, Pacific Bell, Quicknet Technologies, Siemens, Telios, TRI Inc, VCON, and Zydacron.

The enabling technologies have matured and now allow widespread deployment of interactive desktop multimedia communications applications. Key requirements for successful adoption will be the ability to provide dedicated bandwidth isochronous connections that are configurable and allocable according to ITU, IEEE, and ISDN standards.

**FIGURE 2**

Code Bits	Symbol	Assignment
Data Symbols		Tag Bit = 0
11110	0	0000
10010	1	0001
01010	2	0010
11010	3	0011
10100	4	0100
10110	5	0101
01110	6	0110
11100	7	0111
01001	8	1000
10011	9	1001
01011	A	1010
11011	B	1011
10101	C	1100
10111	D	1101
01111	E	1110
11101	F	1111
Control Symbols		Tab Bit = 1
11111	I	No Carrier (Idle)
11001	S	No Data
01100	U	Unaligned Data
11000	J	Start of Frame 1
10001	K	Start of Frame 2
Reserved/Invalid Code Assignments		
01101	R	Reserved*
00000	R	Reserved*
00100	R	Reserved*
00111	R	Reserved*
00001	V	Invalid
00010	V	Invalid
00011	V	Invalid
00101	V	Invalid
00110	V	Invalid
01000	V	Invalid
10000	V	Invalid

\*These code assignments are not used and are invalid.

**IsoEthernet employs 4B/5B symbol encoding; also shown are the data and control-code symbols that are employed in this technology.**

This connection capability must be able to upgrade existing LAN installations and to coexist without disrupting existing LAN data traffic.

EDN

### Author's biography



Richard Brand is strategic marketing manager for National Semiconductor Corp (Santa Clara, CA), where he has been employed for 17 years. He has a bachelor's degree from Stanford University, Stanford, CA, and is a member of the IEEE 802 LAN/MAN Committee and president of the Multimedia Communications Forum.

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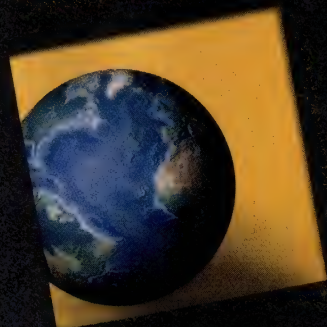


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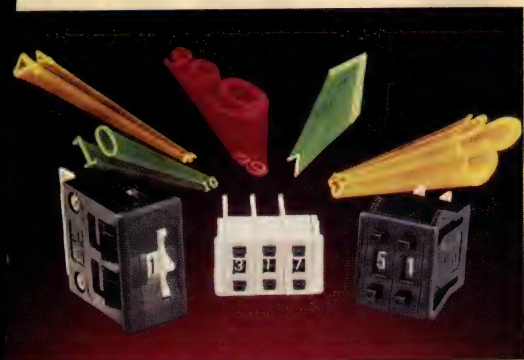
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## ► SWITCHES ► RELAYS



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**C&K Components Inc.**, Watertown, MA. (617) 926-6400.

**Circle No. 433**



### EUROPEAN-STYLED SWITCHES AND INDICATORS.

The European-styled rocker switches, pushbutton switches, and indicators have contoured corners and matte finishes. The switches are available nonilluminated or illuminated with incandescent, neon, or fluorescent lamps. They are designed for front-panel, snap-in mounting. The switches suit use in ac and low-voltage dc applications and have current ratings as high as 20A. Models are available with one through four poles in both maintained and momentary circuits. Prices range from \$0.60 to \$3 (1000). **Eaton Corp., Aerospace and Commercial Controls**, Milwaukee, WI. (414) 449-7326.

**Circle No. 435**



### AUTOMOTIVE RELAYS OFFER COMPACTNESS AND HIGH POWER RATING.

The FBR510/520 twin relay series has a 25A current rating. The relays suit automotive applications requiring forward and reverse motor controls, such as door locks, power windows, retractable outside mirrors, power antennae, and adjustable steering wheels. The relays combine two independent 1 Form C relays into one package measuring 24.3 mm long×16.5 mm wide×14.5 mm high. The FBR510 series has a 0.3-mm contact gap, and the FBR520 series has a 0.6-mm contact gap for increased current shut-off capability at 20V or greater. Each relay has a maximum interrupt rating of 35A and an operating temperature range of -40 to +85°C. Contact voltage drop at 12V dc with 2A current is 100 mV or less. \$2.04 (10,000). **Fujitsu Microelectronics Inc.**, San Jose, CA. (408) 922-9000.

**Circle No. 434**



## COMPONENTS

- ▶ SWITCHES
- ▶ RELAYS



### SOLID-STATE RELAYS AVAILABLE IN PCMCIA-COMPATIBLE FLATPACK.

These low-profile, 0.080-in.-thick flatpacks are available for all two-pole, solid-state relay designs. They include 2 Form A, 2 Form B, 1 Form A/1 Form B, and 1 Form C. The TS Series solid-state switch with combination hook-switch and ring detection is also available in the flatpack. The relays provide blocking as high as 400V ac or dc, load currents as high as 250 mA, and on-resistance as low as 7Ω. The relays are also available with input/output isolation of 3750V rms. The TS117P flatpack relay costs \$3.13 (10,000).

**CP Clare Corp, Solid State Products Division**, Wakefield, MA. (617) 246-4000.

**Circle No. 436**



### 7-MM ROTARY DIP SWITCHES SAVES SPACE.

The MRD Series rotary DIP switches require 40% less pc board space than ordinary rotary DIP switches. The switches use gold-plated contacts for reliability and are process-sealed to prevent contamination from flux and solder washing. The rotary switches are available in eight standard configurations, including BCD, hexadecimal, BCD-complement, hexadecimal complement, surface-mount, and plated through-hole versions. Typical price is \$1.86 (10,000). **Augat Inc**, Attleboro Falls, MA. (508) 699-9800.

**Circle No. 437**



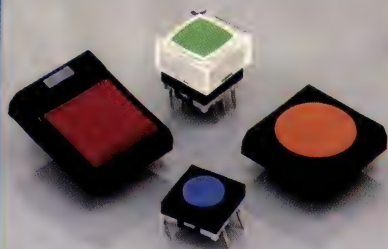
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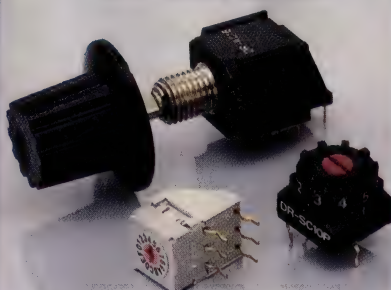


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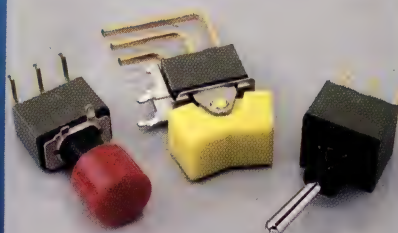
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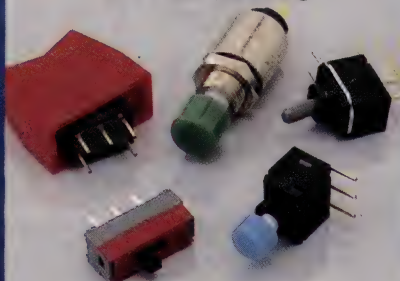
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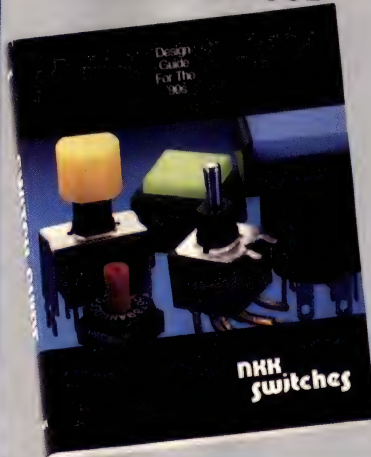
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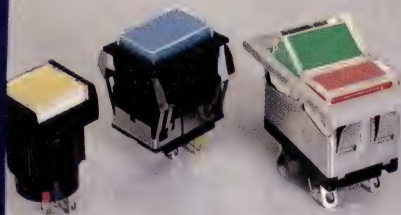


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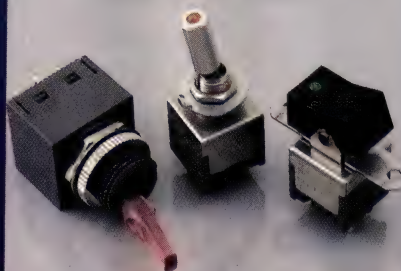
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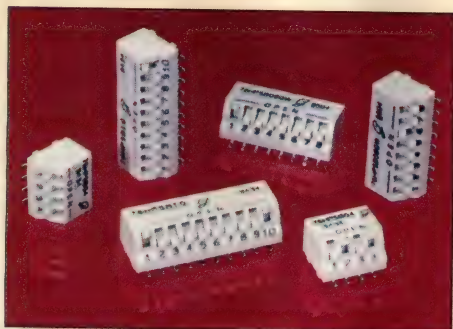
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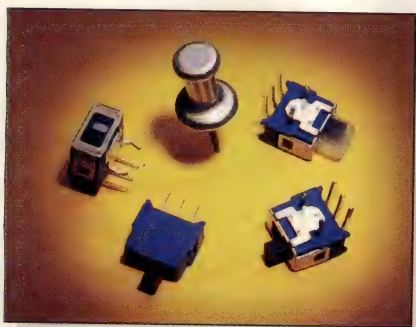
- ▶ SWITCHES
- ▶ RELAYS



### SURFACE-MOUNT, SIDE-ACTUATED DIP SWITCHES.

The surface-mount Piano-DIPs allow operator actuation when they are mounted at the edge of closely racked pc boards. The side-actuated switch assemblies are available with four, eight, or 10 switches. Typical price is \$1.60 (1000). **Grayhill Inc.**, LaGrange, IL. (708) 482-2132.

**Circle No. 439**



### SUBMINIATURE SLIDE SWITCHES FIT TIGHT APPLICATIONS.

The TG Series spdt models have a body size measuring  $0.397 \times 0.196 \times 0.358$  in. The switch series comprises six process-compatible, washable models and six standard non-washable models. The switches suit vertical or horizontal pc-

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### CELL-BYPASS SWITCH PROTECTS AGAINST BATTERY-CELL FAILURE.

The Model 1181 cell-bypass switch depends on a separate circuit to sense cell failure and send a command to the switch. The signal causes the switch to activate, closing the bypass circuit to ensure continued battery service. The switch provides long-term protection in spacecraft battery cells and other applications that cannot tolerate battery-cell failure. The 3-oz switch is rated for a 200A continuous current and 350A momentary overload. Actuation time is <25 msec at 5A. The switch costs \$550 (250).

**G&H Technology Inc.**, Camarillo, CA. (805) 484-0543. **Circle No. 440**

60,000 cycles for the two-position models and 30,000 cycles for the three-position models. The TG36P0-0000 costs \$1.44 (1000). **Mors/Asc**, Wakefield, MA. (617) 246-1007.

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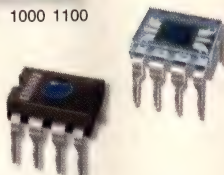
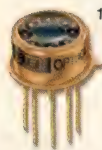
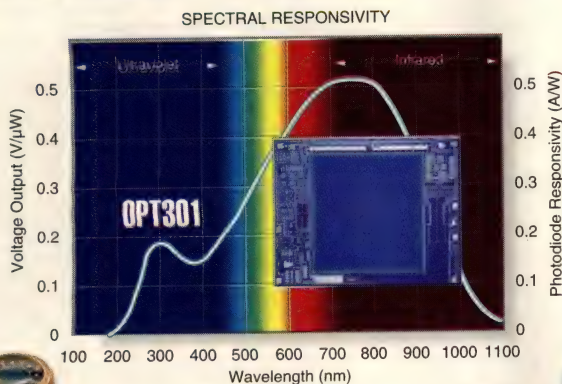
Reader No. 137

## Versatile IC Delivers Wide Bandwidth at High Gains

**OPT211** is a monolithic photodiode with on-chip FET-input transimpedance amp—with an external 1M $\Omega$  resistor, bandwidth is 150kHz—with a 100M $\Omega$ , it's 13kHz. It's your best choice for high sensitivity (low light levels) with high speed. Key specs are: 0.09" x 0.09" photodiode, 0.45A/W (650nm) responsivity, 2mV dark errors, 400 $\mu$ A quiescent current, and  $\pm$ 2.25 to  $\pm$ 18V supply range. Available in a clear plastic 8-pin DIP.

Reader No. 136

## Low Cost



## Simplifies Optical Front-End Designs

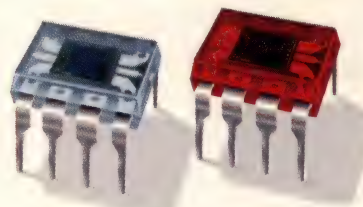
**OPT202**, **OPT209**, and **OPT301** are low cost solutions for precision instrumentation, scanning, and sensing applications. All share common features: the large, sensitive photodiode; a 1M $\Omega$  feedback resistor; high responsivity, 0.45A/W; low dark errors; and a wide  $\pm$ 2.25 to  $\pm$ 18V supply range. **OPT209** provides excellent performance for general purpose applications at 16kHz. **OPT202**'s bandwidth is 50kHz—ideal for pulsed-light applications such as barcode scanners. Both are packaged in 8-pin clear plastic DIPs. **OPT301** provides improved ultraviolet response—excellent for spectrophotometers and fluorescence detectors—it's packaged in a hermetic TO-99 and operates over the  $-55/+125^{\circ}$ C MIL temperature range.

Reader No. 138

## New

## LOW COST SINGLE SUPPLY

**OPT101**



## Photodiode/Transimpedance Amplifier

**OPT101** combines a high performance photodiode, micro-power transimpedance amp and 1M $\Omega$  feedback resistor on a single chip. Designed for single or dual supply operation, it's ideal for battery operated equipment. Power supply current is 120 $\mu$ A and single supply operation extends from 2.7V to 36V. Key specs are: 14kHz bandwidth with internal 1M $\Omega$  feedback resistor, 0.45A/W (650nm) responsivity, and 0.01% nonlinearity. **OPT101** is now available in a new, "optically friendly", innovative package—a 5-pin SIP—that allows light to enter from the "side" of system boards rather than from perpendicular sources. It's ideal for industrial applications—medical and laboratory instrumentation, glucometers, bacteria analyzers, gas detectors, position and proximity sensors, photographic analyzers, smoke detectors, currency validators, and automatic room lighting controllers. Available in a clear and red plastic 8-pin DIP and 5-pin vertically mounted SIP.



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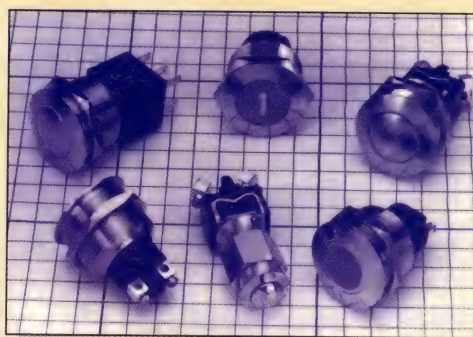
► SWITCHES  
► RELAYS

### MINIATURE ROTARY ENCODED SWITCHES.

The Series 26 rotary switches measure 0.5 in. in diameter and require  $<3/8$ -in. depth behind the mounting panel.

Eight- and 16-position switches are available with BCD outputs, and 16-position switches are also available with Gray code outputs.

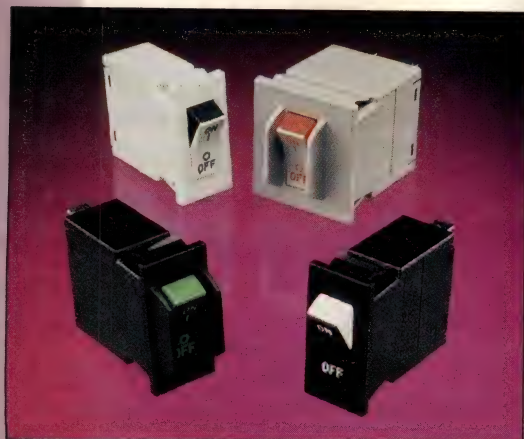
Adjustable stops pins let you select the amount of rotation and the code outputs to customize the switches for fewer positions. The \$7 (100) electromechanical switches are an alternative to electronic digital encoders and thumb-wheel switches. **Grayhill Inc.**, LaGrange, IL. (708) 354-1040. **Circle No. 443**



### VANDAL-RESISTANT PUSHBUTTON SWITCHES.

The AV and AV Monoblock Series pushbutton switches withstand abuse—even vandalism—in applications such as automatic-teller machines, building-access control panels, security panels, and unsupervised public kiosks. The impact-resistant models have an antijamming design to prevent insertion of foreign parts between the pushbutton actuator and body of the switch. Impact resistance meets the requirements of NFC 20010 & CECC. Dust and water sealing is also available for these switches. The switches are rated for 10,000 cycles. From \$5.95 (1000).

**Mors/Asc**, Wakefield, MA. (617) 246-1007. **Circle No. 444**



### MINIATURE MAGNETIC CIRCUIT BREAKERS.

The M-Series Visi-Rocker circuit breakers are available in single- or double-pole configurations. The switches have two-color actuators, providing a visible indication of the status of the breaker, whether on or tripped/off. The nonilluminated circuit breakers are rated for up to 25A and 250V ac or 65V dc. Other features include

snap-in mounting to fit industry-standard cutouts, wiping contacts to reduce carbon buildup, and optional rocker guards to prevent inadvertent actuation of rockers. Prices for the miniature circuit breakers start at \$5.65 (500). **Carlingswitch**, Plainville, CT. (203) 793-9281.

**Circle No. 445**





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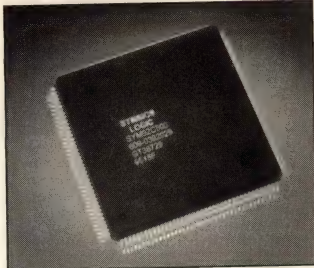
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psec unloaded and dissipates 0.18 mW. **Vitesse Semiconductor Corp.**, Camarillo, CA. (805) 388-3700.

**Circle No. 365**



**Full-duplex switched Ethernet in a single chip.** The SYM92C500 Ethernet device includes the switching fabric, integrated Media Access Controller (MAC), Manchester encoder/decoder, Attachment Unit Interface (AUI), and 10Base-T transceiver on a single chip. Advanced functions such as cut-through and store-and-for-

ward modes aid performance in switching applications including hubs, routers, and network accelerators. The device provides an internal high-speed-bus architecture, which allows you to construct stackable medium to large switches. The SYM92C500's 640-Mbps bus supports multiple half- and full-duplex connections at both 10 and 100 Mbps. The device is housed in a 160-pin PQFP and costs \$40 (1000). Samples are available now, and production quantities are planned for September. **Symbios Logic Inc.**, Fort Collins, CO. (970) 223-5100.

**Circle No. 366**

**Reed-Solomon Viterbi forward-error-correction IC operates to 62 Mbps.** The AHA4210 encoding-decoding IC costs \$35 (1000). It conforms to the

MPEG-II transport layer protocol specified by the ISO/IEC standard and the FEC requirements of the European Broadcasting Union Digital Video Broadcasting DT/8622/DVB and DT/8610/111-B specifications. For flexibility, the device has programmable code rates, block size, and interleave depth. **Advanced Harvard Architectures Inc.**, Pullman, WA. (509) 334-1000.

**Circle No. 367**

**Mixer circuits for wireless systems have operating frequencies to 2.5 GHz.** The PMB 2331 is a 2.7 to 4.5V, 1.6-mA Gilbert cell mixer with highly isolated RF, LO, and IF ports; its noise figure is 8 dB. The device costs \$1.23 (10,000). The PMB 2332 is a mixer and low-noise amplifier with all the features of the PMB

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**CIRCLE NO. 30**



2331. It has a 10-dB gain and a noise figure of 3.3 dB at 2.5 GHz. The device costs \$1.75 (10,000). The PM2333 is a mixer-and-driver amplifier circuit with all the features of the PMB 2331. The driver amplifier has a 10-dBm output power at 1-dB compression; it costs \$1.75 (10,000). **Siemens Components Inc, IC Division, Cupertino, CA. (408) 777-4500.**

**Circle No. 368**

**4-Mbit EEPROM has 150-nsec access time and 300- $\mu$ A standby current.** The AT28C040 is organized as 512k $\times$ 8-bit words in 256 pages. Page-write cycle time is 10 msec. Active current is 80 mA. The device is available in a 32-pin flatpack, a sidebraced package, and a 44-pin LCC; it costs from \$1000 (2000). **Atmel Corp, San Jose, CA. (408) 441-0311.**

**Circle No. 369**

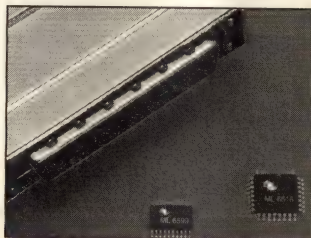
**Multimedia sound chips for Windows 95.** The 82C924 is a Plug-and-Play-compatible 16-bit sound controller intended for business-audio, educational, entertainment, and multimedia applications. The chip is a drop-in replacement for the company's 82C929 sound controller. The device is housed in a 100-pin PQFP and costs \$9 (10,000). The 82C941 is an advanced sound synthesizer with a wave-table synthesis engine intended for PC sound cards, musical instruments, Karaoke machines, and MIDI modules. The device is housed in a 100-pin PQFP and costs \$15 (10,000). **Opti Inc, Santa Clara, CA. (408) 980-8178.**

**Circle No. 370**

**32- and 48-port program-mable interconnect devices.** The IQ32B, with 32 I/O ports, and the IQ48, with 48 I/O ports, operate at a clock rate of 133 MHz and

have a flow-through delay of 5 nsec. You program switch-matrix connections using internal SRAM cells and registers. The devices let you incrementally alter the configuration on the fly, which suits them for dynamically reconfigured systems. The IQ32B costs \$5.79 (10,000); the IQ48 costs \$8.85 (10,000). Both parts are sampling now, and production is scheduled for the third quarter. **I-Cube Inc, Santa Clara, CA. (408) 986-1077.**

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**SCSI-bus interface chips make SCSI peripherals hot-swappable.** The ML6599 terminates nine SCSI lines; the ML6518 terminates 18 SCSI lines. The devices let you design disk drives and other peripherals so that they may be hot-swapped in or out of a system without delays from powering down. They use a circuit that prevents current flow across the SCSI lines until the connector is seated. The chips also have active circuits that eliminate transmission-line noise and improve the reliability of data transfers between peripherals and computers. The ML6599 costs \$1.89 (1000) in a 20-pin SOIC and \$1.93 (1000) in a 20-pin TSSOP. The ML6518 costs \$3.41 (1000) in a 32-pin TQFP. **Micro Linear Corp, San Jose, CA. (408) 433-5200.**

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**Development system helps you add serial EEPROM to  $\mu$ P and  $\mu$ C systems.** The XK84 development system includes an EISA bus add-in card, soft-

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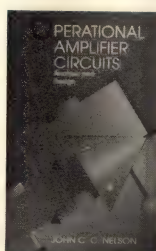
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ware, and three prototype X84041 EEPROMs. The development kit is designed to help evaluate and debug prototype designs using the company's MPS nonvolatile serial-memory devices, which are capable of operating on byte-wide parallel bus systems. Unlike memory devices that are limited to Microwire, I<sup>2</sup>C, or SPI serial interfaces, the MPS devices let you reallocate I/O ports. The development system costs \$84. Xicor Inc, Milpitas, CA. (408) 432-8888. **Circle No. 373**

**16×16 crosspoint switch operates at data rates up to 1.2 Gbps.** The TQ8015-Q 16×16 crosspoint switch features a nonblocking architecture based on 16 fully independent 16:1 multiplexers. It uses a differential data path to provide a maximum of 150 psec p-p jitter and channel-to-channel propagation delay skew of 500 psec. The ECL device requires ±5V supplies and is housed in a 132-pin MQFP package. The TQ8017-Q performs the same function but uses a PECL data interface and operates from a single 5V supply. Either device costs \$100 (1000). Triquint Semiconductor Inc, Beaverton, OR. (503) 644-3535. **Circle No. 374**



**Extended temperature range op amps feature rail-to-rail I/O range.** The LMC6492 dual and the LMC6494 quad op amps are guaranteed for operation from -40 to +125°C and operate to within 20 mV of the supply rails with a 100-kΩ load. The devices have a maximum input-bias current of 200 pA over the full temperature range. Typical supply current is 500 μA per channel. The op amps are designed for automotive applications, including transducers and pressure, oxygen, temperature, and speed sensors. The devices operate from 5 to 15V supplies and are available in eight-pin DIP, eight-pin SO, 14-pin DIP, and 14-pin SO packages. From \$1.85 (1000). National Semiconductor Corp, Santa Clara, CA. (800) 272-9959. **Circle No. 375**

**PLL clock drivers offer six and eight outputs.** The QS5917 has eight TTL outputs and is a pin-for-pin replacement for the MC88915. It offers frequency multiples of times-2, divide-by-2, and inverting. The device is available in 28-pin QSOP and PLCC packages and costs \$9.94 (5000). The QS5930 has five Q outputs and one divide-by-2 output. Three versions are available with maximum frequencies

of 50, 66, and 75 MHz. The QS5930 is available in a 20-pin QSOP and costs \$6.40 (5000). Quality Semiconductor Inc, Santa Clara, CA. (408) 450-8080. **Circle No. 376**

**Dual-band PLL frequency synthesizer has ADC and frequency counter.** The MC145173 is a single chip CMOS synthesizer with a four-

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wire serial interface for use in AM-FM broadcast receivers, long- and short-wave receivers, VHF scanners, and other RF applications from 550 kHz to 130 MHz. Two on-chip, 6-bit ADCs let you monitor two voltage levels in a radio application. A 22-stage counter accepts two IF signals for a seek or scan function on radio receivers. In addition to four general-purpose digital outputs, the device allows direct interface to the

company's SPI data port, compatible with 8-, 16-, and 32-bit microcontrollers. Operating from 4.5 to 5.5V, the device has a maximum operating-mode supply current of 12 mA. Standby current is 30  $\mu$ A. The device costs \$2.04 (5000) and comes housed in a 24-lead SOG (small-outline-gull-wing) package. **Motorola Microcontroller Technologies Group**, Austin, TX. (800) 422-6323.

**Circle No. 377**

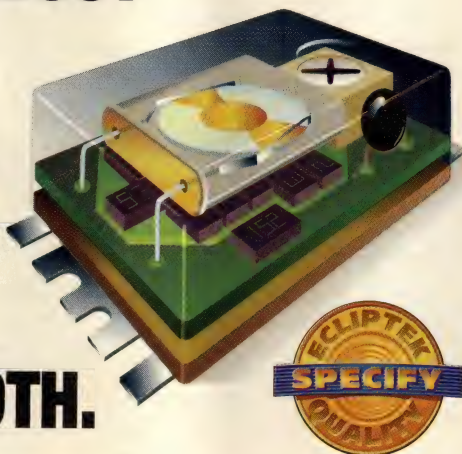
**Frequency timing generators for multimedia sound systems.** The ICS9120-08/09 generate the standard clock frequencies used by sound-system audio synthesizers and high-performance coders-decoders. The devices generate the three standard audio clocks of 16.9344, 24.576, and 33.868 MHz. The generators also provide a buffered 14.31818-MHz reference clock output. Output frequencies have 0.01% accuracy and <85-psec, 1-sigma jitter. Housed in an eight-pin, 150-mil SOIC package, the devices cost \$1.40 (10,000). **Integrated Circuit Systems Inc.**, San Jose, CA. (408) 297-1201.

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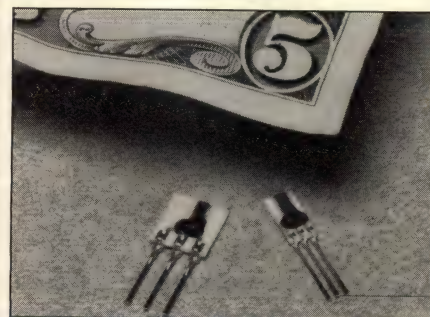
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**Humidity sensor IC.** The IH-3605-B measures relative humidity from 0 to 100% over a temperature range of -40 to +185°F. The three-pin SIP operates from a 5V supply and provides a 0.8 to 4.0V linear output, corresponding to 0 to 100% relative humidity. Two-point calibration establishes  $\pm 2\%$  accuracy. The sensor resists contaminating vapors and is unaffected by water condensation. It costs \$7 (OEM). **HyCal, El Monte, CA.** (818) 444-4000.

**Circle No. 379**

**8:1 and dual 4:1 multiplexers offer high speed and withstand spikes from -35 to +50V.** The 8:1 ADG438F and the 4:1 ADG439F are fault-protected multiplexers with a 400 $\Omega$  maximum on-resistance, a maximum turn-on time of 250 nsec, and a maximum turn-off time of 150 nsec. The CMOS analog multiplexers are available in DIP and 0.15-in. SOIC packages. The devices are specified for operation from -40 to +105°C and cost \$3.69 (1000). **Analog Devices Inc.**, Wilmington, MA. (617) 937-1428.

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**Single-polarity tracking regulator functions as power op amp.** The CS-8181 tracking regulator is a high-gain



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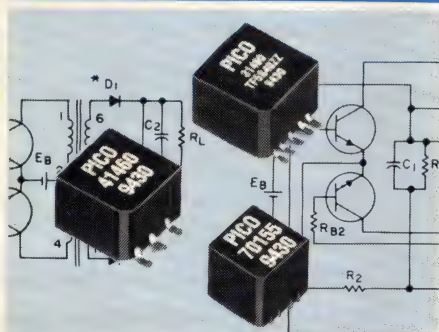
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noninverting operational amplifier. The device's positive output voltage tracks its reference input within  $\pm 5\text{mV}$ . The output voltage may be set to any value up to the input voltage, using a resistive voltage divider. The device operates over a 5 to 30V range and has a 0.6V dropout voltage at its rated 150-mA output current. It is fully protected against short circuits in the load, over-voltage, and overtemperature. In standby mode, the device draws a maximum of 1 mA. It operates from  $-40$  to  $+125^{\circ}\text{C}$  and is available in a five-lead TO-220, eight-lead plastic DIP, and a 16-lead small-outline wide DIP. \$1.37 (10,000). **Cherry Semiconductor Corp.**, East Greenwich, RI. (401) 885-3600.

Circle No. 381

**Dual-output dc/dc converter fits on PCMCIA cards.** The MAX624 provides a fixed 5V  $\pm 4\%$  output at 200 mA and an adjustable auxiliary output for voltages, ranging from the input voltage to 30V. The converter accepts an input from 3 to 5.5V and has a typical efficiency of 85% for loads from 20 to 200 mA. Shutdown current is 40  $\mu\text{A}$ . The chip features independent soft starts for each converter and an optional inrush current limiter, allowing for hot insertion of cards without causing system glitches. The converter starts at \$5.25 (1000) and comes housed in a 16-pin-narrow SO package. **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087.

Circle No. 382

**16-Mbit DRAMs have 32-bit organization.** These 512k $\times$ 32-bit DRAMs are available in three versions. The TC5118320BJ-60/70 is a 5V device with 60/70-nsec access time, offering fast page-mode operation. It is housed in a 70-pin SOJ package. The TC5118325BJ-60/70 is a 5V device with 60/70-nsec access time, offering extended-data-out (EDO) mode operation. It is also housed in a 70-pin SOJ package. The TC51V16325BFT-70 is a 3.3V device with 70-nsec access time, offering EDO mode operation. It is housed in a 70-pin TSOP package. Samples cost \$135 (1000). **Toshiba America Electronic Components Inc.**, Irvine, CA. (800) 879-4963.

Circle No. 383

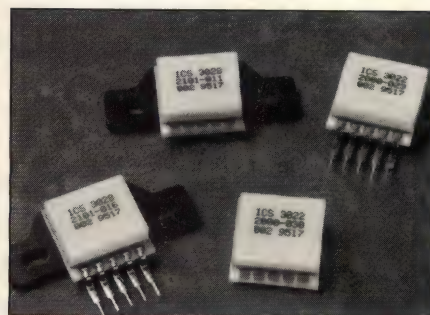
**Serial EPROM family offers 10-MHz speed.** The 37LVXX serial EPROM family with 10-MHz speed provides fast boot-up for SRAM-based FPGA applica-

tions, computer BIOS, video games, and digital signal processing. The devices in the family operate between 3 and 6V. The serial EPROMs are internally organized in a  $\times 32$  configuration and have a maximum read current of 10 mA at 5V and standby current of 100  $\mu\text{A}$  at 5V. The serial memories are available with capacities of 36, 64, and 128 kbits. The devices are available in eight-pin DIP, eight-pin SOIC, and 20-pin PLCC packages. The 37LV36/PDIP costs \$2.87 (1000). **Microchip Technology Inc.**, Chandler, AZ. (602) 786-7200.

Circle No. 384

**Quad analog switches operate from 3 to 10V.** The break-before-make ALD4201 and the make-before-break ALD4202M can operate from  $\pm 1.5$  to  $\pm 5\text{V}$  or from 3 to 10V. Switched signals can range from rail-to-rail levels. Typical on-resistance ranges from 90 $\Omega$  for  $\pm 5\text{V}$  supplies to 500 $\Omega$  for 3V supplies. The switches are available in 16-pin DIP or SOIC packages and cost \$1.83 (100). **Advanced Linear Devices**, Sunnyvale, CA. (408) 747-1155.

Circle No. 385



**General-purpose accelerometers provide mounting flexibility.** The Model 3022 accelerometer is designed for adhesive mounting, and the Model 3028 is designed for mechanical mounting. The micromachined sensors are designed for OEM applications, including vibration monitoring, motion control, tilt monitoring, shock and transportation recorders, structural analysis, and vehicle instrumentation. In the United States, both models cost \$69 (100). Ranges of 10g and below cost \$81 (100). **EG&G IC Sensors**, Milpitas, CA. (408) 432-1800.

Circle No. 386

**Complex PLD offers 256 macrocells and a 83.3-MHz system speed.** The MACH465-12 has 10,000 gates, providing 256 macrocells and 384 flip-flops.



Each of the macrocells provides capacity for up to 20 product terms and includes XOR logic. The device includes 146 inputs, 128 of which have dedicated input registers. It also accommodates 5V in-circuit programming and has JTAG test provisions. The MACH465-12YC costs \$144.81 (1000). Advanced Micro Devices Inc, Sunnyvale, CA. (408) 749-5703.

Circle No. 387

mized for 3.3V, the library's I/O cells can tolerate 5V input signals. The library provides more than 450 digital core cells and 180 core functional blocks. The delay for a one-input NAND gate with a fan-out of 2 is 140 psec. The process supports designs with more than 400,000 gates. Baseline NRE is \$50,000 for 20,000 gates and \$120,000 for 100,000 gates. Symbios Logic Inc, Fort Collins, CO. (970) 223-5100.

Circle No. 390

**Unified system/display controller.** The W464 chip set combines a 64-bit GUI controller, 135-MHz RAMDAC, and 486-compatible PCI core logic. The 64-bit-wide unified memory subsystem can be used for both main CPU memory and as a graphics frame buffer. The chip set costs \$43.50 (10,000). Weitek Corp, Sunnyvale, CA. (408) 738-8400.

Circle No. 391



**8-bit ADC operates at 20M samples/sec.** The ML6401 includes sample and hold, input amplifier, and reference voltage. It is able to maintain 7 bits of effective resolution while converting at 20M samples/sec. The chip is pin-compatible with the industry standard 1175 series ADCs from Sony, Harris, Raytheon, and Micro Power Systems. According to the company, an internal pipelined architecture provides better effective resolution at high speeds and lower input capacitance than competitive converters. The device is available in a 24-pin SOIC or PDIP packages and costs \$6.75 (1000). Micro Linear Corp, San Jose, CA. (408) 433-5200.

Circle No. 388

**Complex PLD family now offers in-system programmability.** The MAX 7000S family provides in-system programmability and JTAG boundary-scan testing. The family is pin-out- and programming-file-compatible with the existing MAX 7000 and MAX 7000E devices. The first device, the EPM7128S, will be available in 1996 and has a projected volume price of \$10. Altera Corp, San Jose, CA. (408) 894-7000.

Circle No. 389

**Cell-based library for half- $\mu$ m, 3.3V, triple-level, metal CMOS process.** The VS350 cell-based library is 20% faster than the VS500 library, its 0.76- $\mu$ m predecessor. Although opti-



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<sup>1</sup>Sample suite of GPIB programmed audio measurements included 1) noise measurement (20Hz-22kHz bandpass).

2) 31 point single tone frequency response sweep over 20Hz-22kHz range, and 3) 11 point distortion sweep over 20Hz-22kHz range.

<sup>2</sup>FASTTEST uses multi-tone stimulus and analysis to make the same measurements listed above.

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**Circle No. 420**



**Programmable television-test-signal generator.** The TG2000 signal-generation platform has a modular architecture to meet current signal-generation demands and many anticipated requirements. The system provides reference-quality test signals with functions in the analog and digital domains. Comprehensive test-signal libraries are supplied in all formats and are supplemented by a Windows-based test-signal development program. The base price, including one module, is \$9000, and the complete system costs \$18,000. **Tektronix Inc.**, Beaverton, OR. (800) 835-9433. **Circle No. 421**

**Video-test software simplifies troubleshooting MPEG-2 protocol problems.** The HP MPEG-2 Protocol Viewer for the HP E4200/E4210 Broadband series test systems is designed for network developers, video-server designers, set-top-box designers, and

other video-transmission-equipment designers. The product supports the ISO/IEC 13818-1 systems layer standard for MPEG-2. It runs on the HP E4209A cell-protocol processor module and displays transport-stream and packetized element-stream fields and flags. It also clearly displays field-length errors and supports any number of transport-stream packets encapsulated in ATM Adaption Layer-5 frames. The

software costs \$5550. Hewlett-Packard, Santa Clara, CA. (800) 452-4844, ext 9403. **Circle No. 422**

**Windows NT driver supports IEEE-488.2 applications.** Driver488/NT is an IEEE-488.2 device driver for integrating IEEE-488.2 control into Windows NT applications. When used with the company's 8- or 16-bit PC/IEEE-

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488.2 controller boards, the software provides a dynamic-link-library (DLL) driver, language interfaces for C and Visual Basic, DLL entry points for all other languages, and an interactive control program for application start-up and instrument-communication verification without programming. The software costs \$195. **IOtech Inc.**, Cleveland, OH. (216) 439-4091.

**Circle No 423**

**23-bit data-acquisition system.** The Model 250 23-bit data-acquisition system provides 22-bit monotonicity, linearity at 0.001% full scale, and sample rates over 5 kHz. At the maximum speed of 5400 samples/sec, the effective resolution is 19.5 bits. The sampling successive-approximation converter operates in either a track-and-hold or dc mode. The standard differential input range is  $\pm 5V$ , and the dc common

mode range is  $\pm 11V$ . The converter has six fully differential input channels, expandable to 96 channels. The converter, including enclosure and power supply, costs \$1295. **Lawson Labs Inc.**, Kalispell, MT. (406) 257-5355.

**Circle No. 424**

**Low-cost I/O devices for PC.** The Octa-Port system lets you connect eight I/O boards to a PC, DSP, or microcontroller. The boards include an 18-bit, four-channel ADC (\$139); a four-channel, opto-isolated relay system (\$39, plus \$19 per relay); and an eight-channel digital I/O board (\$39). The system uses a bus interface to the PC printer port (\$39) that connects via cables to the I/O boards. The cables may be up to 50 ft long. **Atlantic Technologies Inc.**, Newtown Square, PA. (610) 356-1070.

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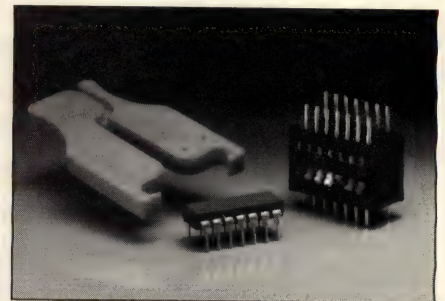
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**Data-acquisition and control software is integrated with Microsoft Office.** MS Office integration and other enhancements are available in version 8.1 of Labtech Notebook, Labtech Notebookpro, DataLab Solution, and GPIBtest Solution; version 5.1 of Labtech control and Labtech Controlpro; and version 2.1 of Real-time Vision. The new integration with MS Office lets you automatically import each acquired data sample and the time



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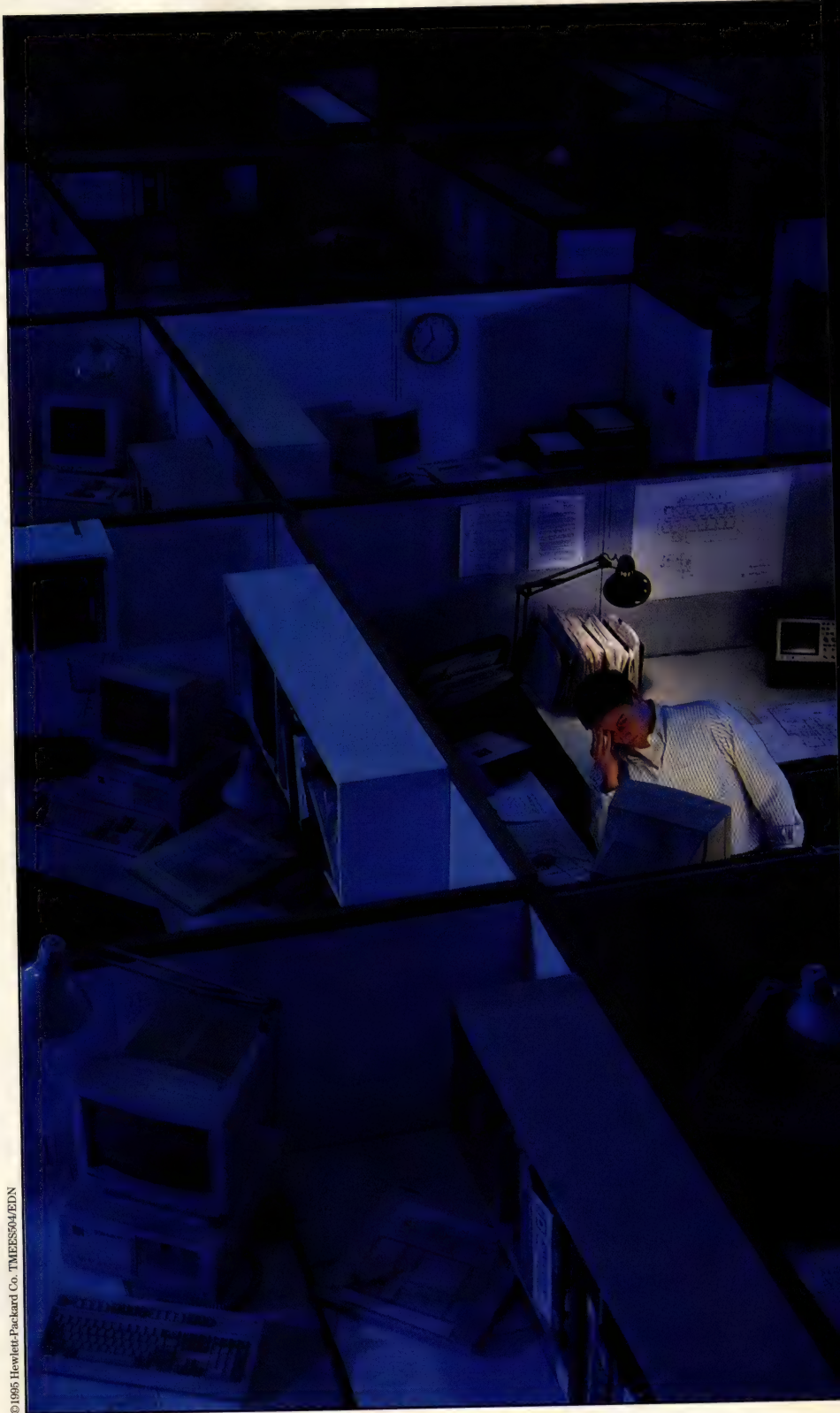
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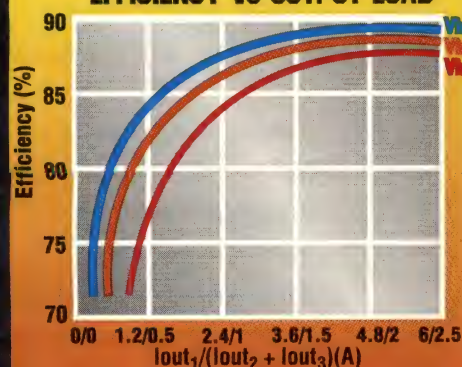
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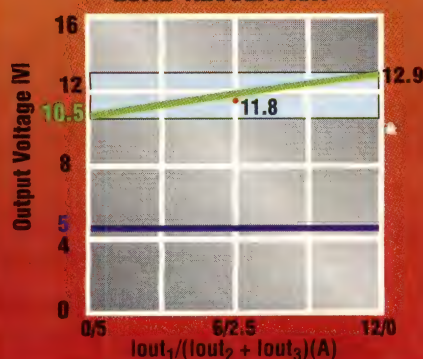
Example below: VKP60MT512

$V_{OUT1} = 5Vdc$   $V_{OUT2} = 12Vdc$   $V_{OUT3} = 12Vdc$

### EFFICIENCY vs OUTPUT LOAD



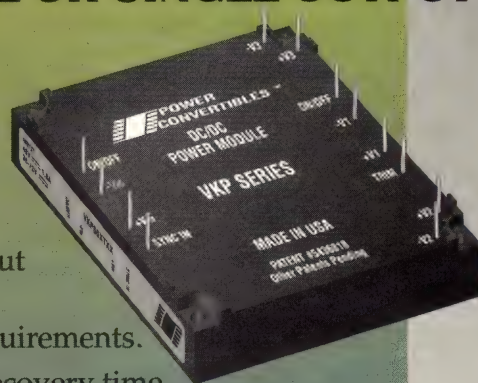
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acquired in real time into MS Excel. All the spreadsheet and charting functions of Excel are available. Upgrade prices range from \$150 for Labtech Notebook to \$495 for Labtech Controlpro. **Laboratory Technology Corp.**, Wilmington, MA. (800) 879-5228.

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**Plotting software adds full 3-D capability.** EasyPlot Version 3 has full 3-D graphing, image plots, 3-D curve fitting, a programming interface, on-line help, and a preference dialog that provides easy access to special features. The tool is able to plot large data sets rapidly, displaying 50,000 points/sec on a 66-MHz 486 system. An animation tool lets you rotate 3-D data in real time. EasyPlot for Windows 3.1 requires 4 Mbytes

of RAM and 800 kbytes of hard-disk space. It costs \$399. EasyPlot for DOS costs \$349. Users of the previous version can upgrade for \$99. **Spiral Software.** Brookline, MA. (617) 739-1511.

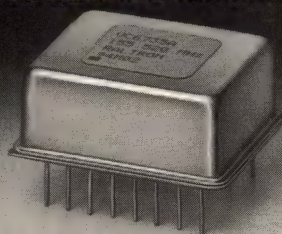
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**Driver provides 1-MHz data-acquisition rate.** The UEIDAQ driver support package for National Instrument's Labwindows/CVI for Windows, when used with the company's WIN-30 PC-based data-acquisition boards, is able to acquire data at 1-MHz until the memory available to Windows is full. The UEIDAQ driver package provides over 100 functions accessible through Labwindows/CVI. The software is free. **United Electronic Industries,** Watertown, MA. (617) 924-1155.

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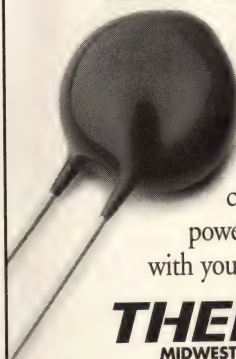
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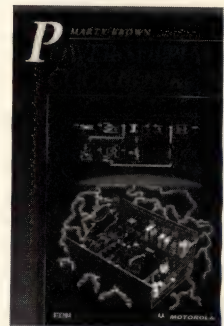
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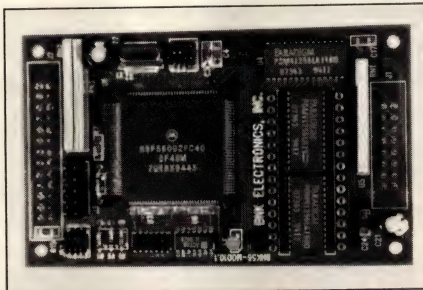
**Fuzzy-logic development tool provides point-and-click prototyping.**

TILShell3.0 Basic Edition lets you design fuzzy-logic systems with a graphical point-and-click scheme in a programless design environment. It has debugging capabilities, providing a 3-D view of control surfaces for fuzzy-system evaluation. The tool allows up to 128 rules and a total of five variables for inputs and outputs; it also provides triangular membership functions. TILShell3.0 Basic Edition costs \$495. Togai InfraLogic Inc, Irvine, CA. (714) 588-3800. **Circle No. 411**

**STD 32 CPU board uses Intel 80C186 processor.** The VL-186-2 has full DOS software compatibility. The 4.5×6.5-in. board has 1-Mbyte SRAM and space for up to 1 Mbyte of flash memory and a flash file system for diskless program storage. The board also has two DOS-compatible COM ports, one parallel port, and floppy and IDE interfaces. The board can run in dual master systems, allowing two of the boards to operate simultaneously in the same card cage without an arbiter card. The board runs from a single 5V supply and is available in either a standard version, operating from 0 to 65°C, or an extended-temperature version, operating from -40 to +85°C. The board costs \$395 (100). Versalogic Corp, Eugene, OR. (800) 824-3163. **Circle No. 412**

**Real-time development tool kit for Windows 95.**

The WinRT Tool Kit is for programmers developing Win32 hardware control applications for Windows 95. The kit lets you write programs to access port I/O, memory I/O, and interrupts directly. Typical applications for the tool kit include data-acquisition systems and process control applications using custom hardware and unsupported I/O cards. The product provides a standard method of hardware control across all supported platforms: Windows 95, Windows NT, Alpha, Mips, and PowerPC. Introductory price is \$295, which includes Windows NT support. Blue-Water Systems, Edmonds, WA. (206) 771-3610. **Circle No. 413**

**DSP module for development and embedded applications.**

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**Development tools for Motorola's ColdFire family.**

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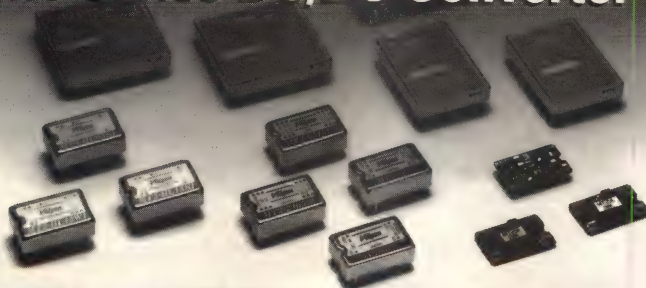


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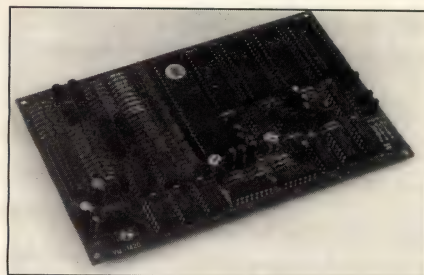
EMBEDDED SYSTEMS

tion, including functions, files, global symbols, and local symbols. The tool lets you set and delete breakpoints, display variables, and track bugs in embedded applications. The instruction-set simulator version starts at \$2000 (for Sun and HP workstations) and \$1500 for use under Windows and Windows NT. **Software Development Systems**, Oak Brook, IL. (708) 368-0400.

Circle No. 415

**Tool simplifies generation of parallel-processing-based DSP applications.** The Pegasus parallel-design environment for Windows works with Texas Instruments' TMS320C40 processors. The tool produces C code from a simple block diagram of your DSP application. It then compiles and optimizes the C code to run as parallel tasks running on multiple DSPs. By using a parallel DSP operating system to control execution and communications, the tool can reallocate tasks to more processors without modifying the system. Unlike block-diagram tools that run as interpreted code, the Pegasus output runs directly as optimized C or assembly code on DSPs. Pegasus for Windows costs \$12,995. **Jovian Systems Inc**, Woburn, MA. (617) 937-6300.

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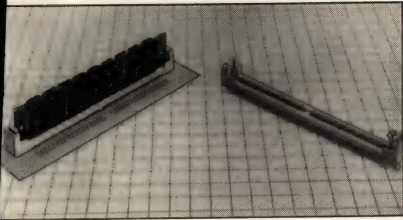


**Self-contained audio board has 17-minute, 20-message capacity.** The VM1420 is a 4.25×6.5-in. board that runs from a single 6 or 12V supply. The board is self-contained and needs no controller to operate. When one of the 20 input-trigger pins on the board activates, the board plays the corresponding message stored in its EPROM. The EPROM holds up to 17 minutes of custom programmed messages. Audio output is 2W into a 4Ω speaker. Standby current is 50 μA when built-in power management circuitry is enabled. Without EPROM, the board costs \$80 (10). **Eletech Electronics Inc**, Industry, CA. (818) 333-6394.

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## 72-PIN SIMM SOCKET AVAILABLE

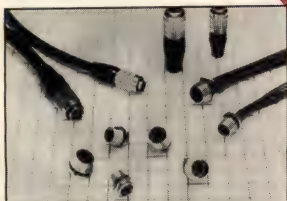


Hirose is providing the SX3, a newly developed SIMM socket suitable for JEDEC standard 72-pin memory module boards with 1.27mm (0.050") spacing. Through the use of FEM analysis, Hirose has molded a latch system which is more durable and cost effective than other products on the market. Contacts on the SX3 provide high performance by utilizing a smooth, rolled-surface design. Pre-loaded contacts provide a stable, reliable force and make the SX3 ideal for personal computers, workstations, computer peripherals, hard disks, office automation equipment and measuring instruments.

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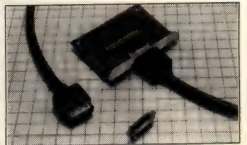
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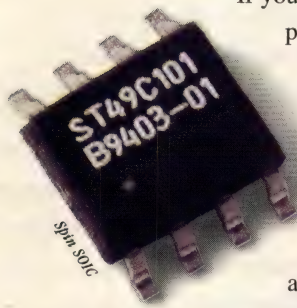
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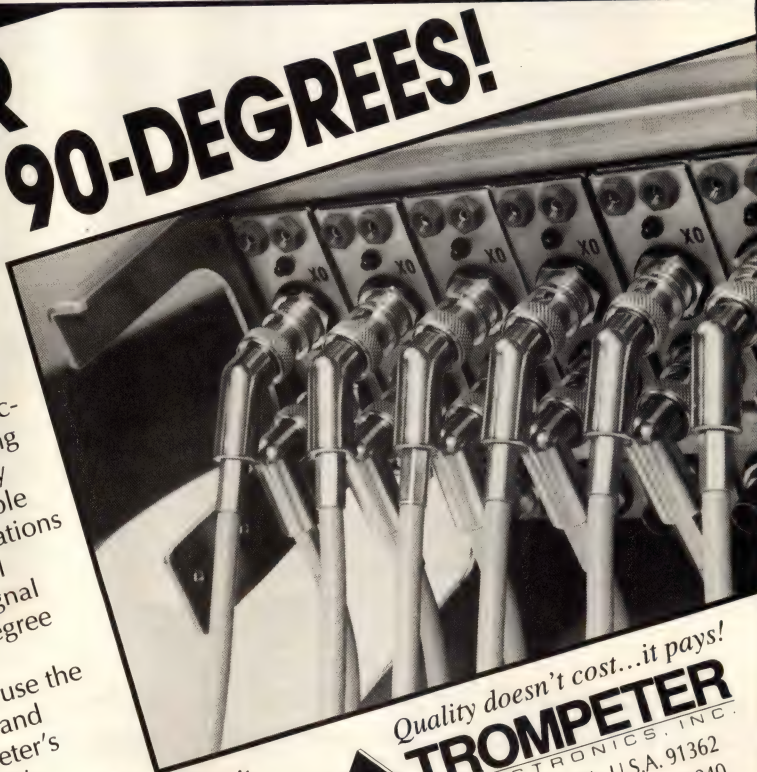
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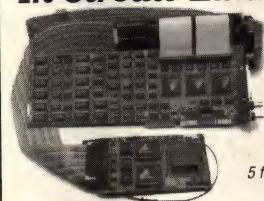
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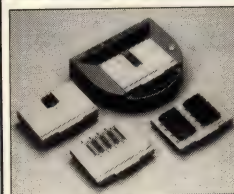
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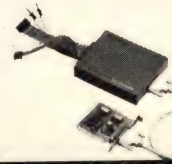
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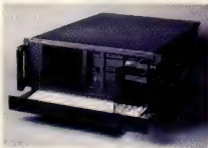
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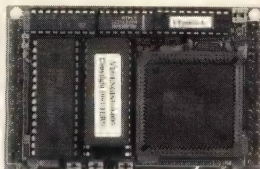
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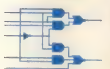
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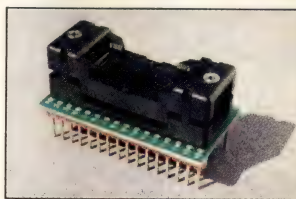
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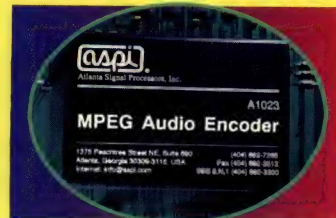
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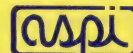
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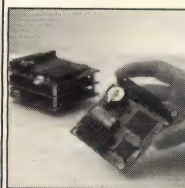


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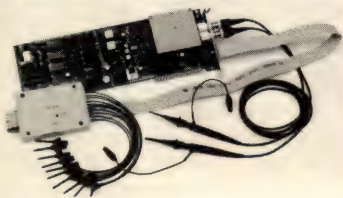
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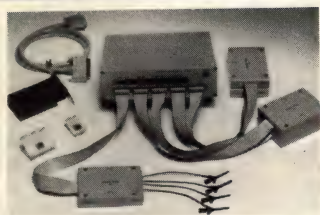
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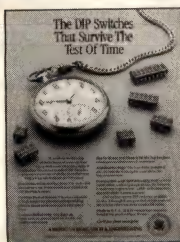
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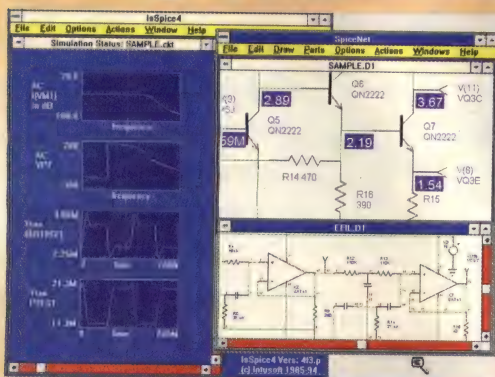


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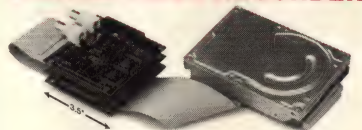
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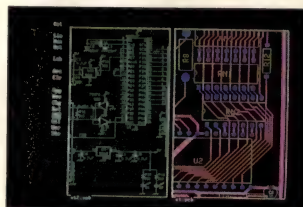
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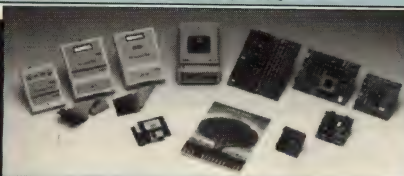


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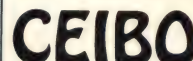
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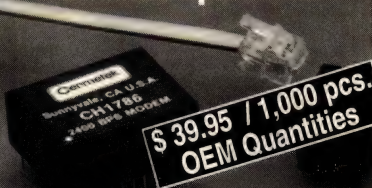
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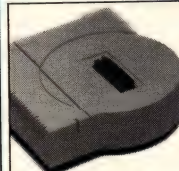
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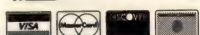
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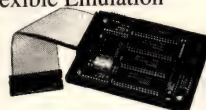


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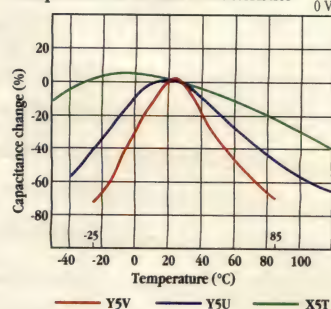


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Rated voltage (V DC)	10V.DC	16V.DC	25V.DC	50V.DC	100V.DC
Capacitance ( $\mu$ F)					
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0.15					
0.22					
0.33					
0.47					
0.68					
1					
1.5					
2.2					
3.3					
4.7					
6.8					
10					
15					
18					
22					

CL Series (Y5V) CL Series (X5T) CT Series (Y5V) CU Series (Y5U)

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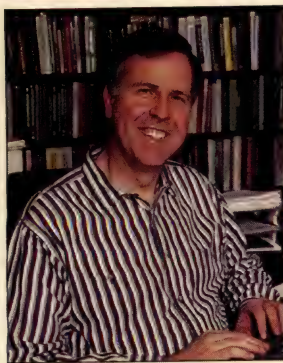
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CIRCLE NO. 120





**DAVID BRUBAKER,**  
FUZZY-LOGIC  
CONTRIBUTING EDITOR

## A fuzzy parable

# Once upon a time...

...there once was a man who wished to build a house. He had built houses before, forming each joint by sawing dovetails, drilling a hole, and pounding a dowel into the hole to secure the joint. Although resulting in strong structures, this approach required much time.

The man had heard about a new technology: nails. They were small, pointed metal stakes that were driven into the wood to secure joints; neither dovetails nor drilling was necessary. The man felt he could save much time if he used nails, so he bought a keg of them.

As an experiment, he placed two boards together and considered how to drive a nail into them. He tried his mallet, which he used to drive dowels into their holes, but the mallet was made of wood, and the head of the nail chewed great holes in the face of the mallet. As the man pondered this problem, a friend approached him.

"What are you doing?" the friend asked.

"I am building a house using nails," the man replied, not without a little pride. "But I do not know how to drive in the nails," he admitted. "The head of my mallet is too soft."

The friend said, "You need a hammer. The head of a hammer is made of steel. You are fortunate, for I am an expert with hammers,

skilled and experienced in their use. I shall buy you one and teach you how to use it."

"If it will help me build my house with nails, please do so," responded the man. The

friend left, returning the next morning with not one, but seven hammers. He laid them out on a piece of canvas and said, "These are hammers."

"Why have you bought so many?" the man asked.

His friend smiled. "You have a large job.

You will need different types of hammers. I like to say 'the right tool for the job.' Let me explain their use." Pointing to the first hammer he said, "This is a standard claw hammer. You will use it most. The claw is used to pull out nails after they have been pounded in." Pointing to the next hammer, he continued, "This is a framing hammer. It is heavier than the standard hammer and is used to drive the larger nails used for framing."

"I bought only one size of nails," the man said.

"We will take care of that," his friend responded, and continued, pointing to the next hammer. "This is a 2-lb hammer. You will use it with the very large nails in your ceiling beams. And this is a roofer's hammer. With this you will put shingles on your roof."

"My house will have a tile roof."

"No matter," said the friend, frowning at the interruption. "This is a finishing hammer. You will use it to set the windows and mount your cabinets. This is a ball-peen hammer. It has a lighter head and a rounded knob at the other end. Finally, this is a tack hammer. It is used to pound in tacks, which are very small nails."

The man bit his lip. "Thank you for all these hammers. I hope I will need them. But now I would like to start building my house. Can you teach me how to do this with a hammer?"

"Yes, of course." The friend picked up the claw hammer and swung it from side to side. After a moment he said, "This hammer is out of balance. I shall need to return it and buy you another one."

"Will it take long?" the man asked. But his friend had not heard him, for he was deep in thought. After a moment, his face brightened. "Better yet, I shall return tomorrow and shall balance the hammer myself."

When his friend was gone, the man picked up the claw hammer in his right hand, held a nail vertically on a piece of wood with his left, and swung the hammer at the head of the nail. He missed and smashed his thumb. When he had finished dancing around, he sat down, nursed his

**“The man picked up the claw hammer with one hand, held a nail vertically on a piece of wood with the other, and swung. He smashed his thumb.”**



thumb, and said to himself, "Perhaps the hammer is out of balance. Or perhaps using a hammer requires greater skill and experience than driving a dowel with a mallet."

The next morning, the man's friend returned with three metal files, two wood files, and two rasps. With great enthusiasm, his friend, apparently an expert with files as well, skilled and wise as to their use, explained the purpose of each. The man listened patiently. Then, using one of the files, the friend started to balance the claw hammer.

To bide his time, the man picked up a stone in his left hand and a nail in his right and attempted to drive the nail into a board with the stone. This time, he smashed his right thumb. While he was dancing around, his friend smiled at him and said, "Now you understand the importance of using the right tool."

Balancing the hammers took the rest of the day. As the sun was setting, his friend

said, "The hammers are now ready. In the morning, I shall return and teach you how to use them."

"I hope so," the man said. The friend had already departed and missed the sarcasm in the man's voice.

The friend arrived early the next morning. The man handed him the now-balanced claw hammer and said, "Please teach me to use this. I would like to start building my house." But instead of accepting the hammer, his friend took a flyer from his back pocket and handed it to the man. "Read this. It describes a power hammer, one that will drive many nails a minute—and all types of nails, as well. You can use it in place of all these hammers. It will allow you to finish your house in far less time. Hammer technology moves quickly."

The man took a deep breath. "I have a house to build," he said. "Using dowels, I would have now been done with

the frame. Instead, nothing has been started. You seem interested only in hammers. I am interested in building my house. I would like to start now."

The friend said, "I am sorry preparing these hammers has taken so long. If you purchase the power hammer, you will still finish your house long before you would have using dowels or these hammers. I promise."

The man was torn, but, after some thought and with some misgivings, he decided he would once more trust his friend—although not completely. "Buy it," he said, "but do not alter it. If the power hammer does not work, you shall return it. Agreed?"

"Agreed. I shall order the hammer tonight," replied the friend, happily, and left. A week later, the friend was

back with the power hammer. With great ceremony, he filled the hammer with framing nails, plugged it in, and flipped the on switch. The power hammer went berserk, spewing nails indiscrimi-

nately. The man

dived for cover and was unhurt, but his friend was not so lucky. In all, he took nine nails in various parts of his body. The man, seeing his friend go down, had risked his own life by leaving his shelter and pulling the cord from the power outlet. The power hammer died.

The man rushed his friend to the hospital, where he was immediately taken into surgery. After several hours, the surgeon emerged. The wounds, the surgeon said, were not fatal, but there would be a long recovery period.

The man visited his friend often, first in the hospital, and then at the friend's home. The man talked of many things, but he did not talk about hammers or about his house. His friend avoided these subjects as well. When he wasn't visiting his friend, the man worked on his house. He sawed dovetails, drilled holes, and secured the joints with dowels, pounding them in with his mallet.

Two months after the accident, his house completed, the man was sawing wood for his wood stove. He crosscut each log into sections, and then cut each section in the direction of the grain numerous times into individual pieces appropriate for his stove. It was hard work, and he had much wood to cut to get ready for the coming winter.

"You have a beautiful house. It is well made."

The man turned to find his friend standing behind him. This was the first time his friend had ventured out since the accident. The man put down his saw and greeted his friend warmly.

"But you did not use nails," continued the friend.

"No," agreed the man. "I did not use nails."

After an awkward pause, his friend changed the subject by asking, "What are you doing?"

"I am sawing wood," the man answered. "We will have a long, cold winter, and I will need much wood. I will saw wood for you as well."

The friend looked at the many log sections that needed to be further cut into stove-sized pieces. "There is a type of hammer called a sledgehammer," he said. "With it and some wedges, you can split these log sections, rather than saw them. Using a sledgehammer and wedges would save you much time and energy."

Sadly, feeling justified, the man invited his friend to leave.

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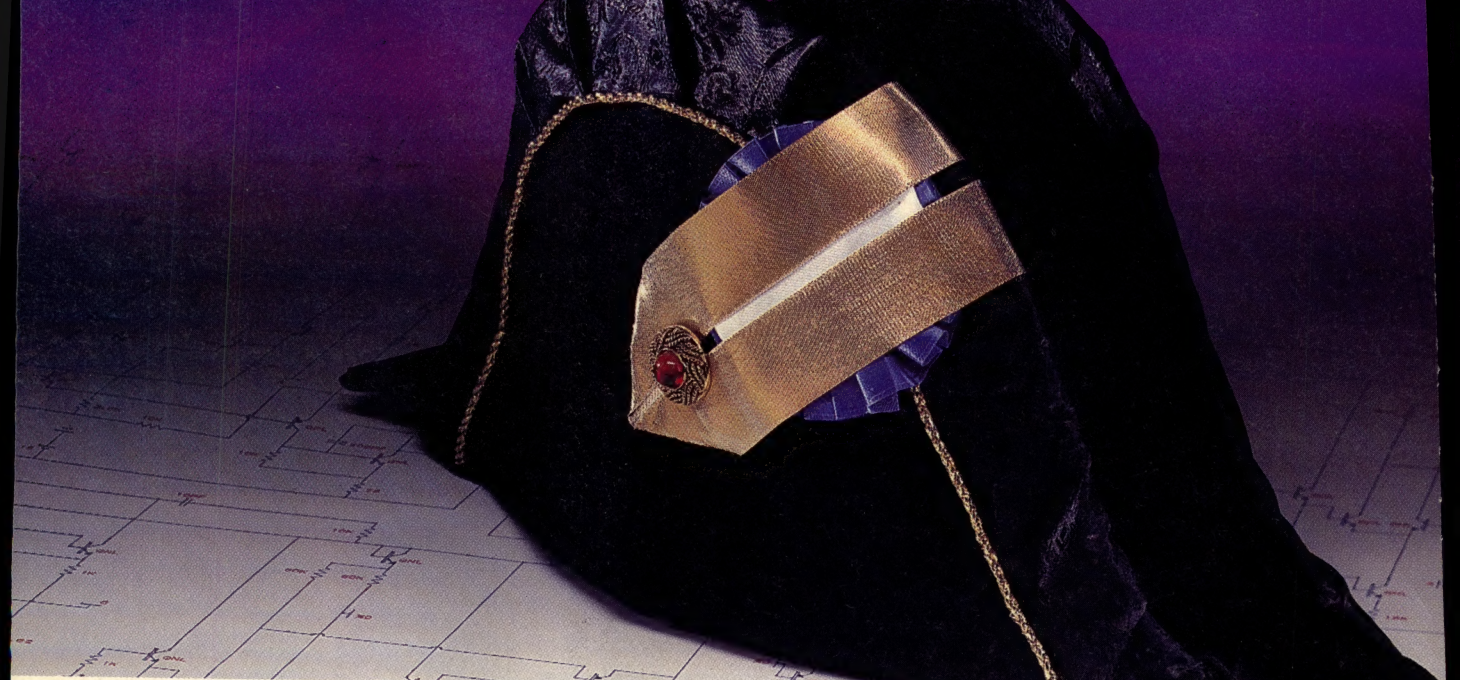
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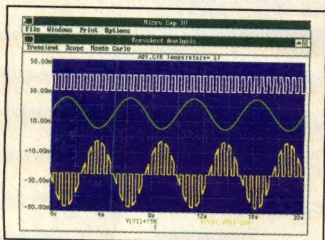


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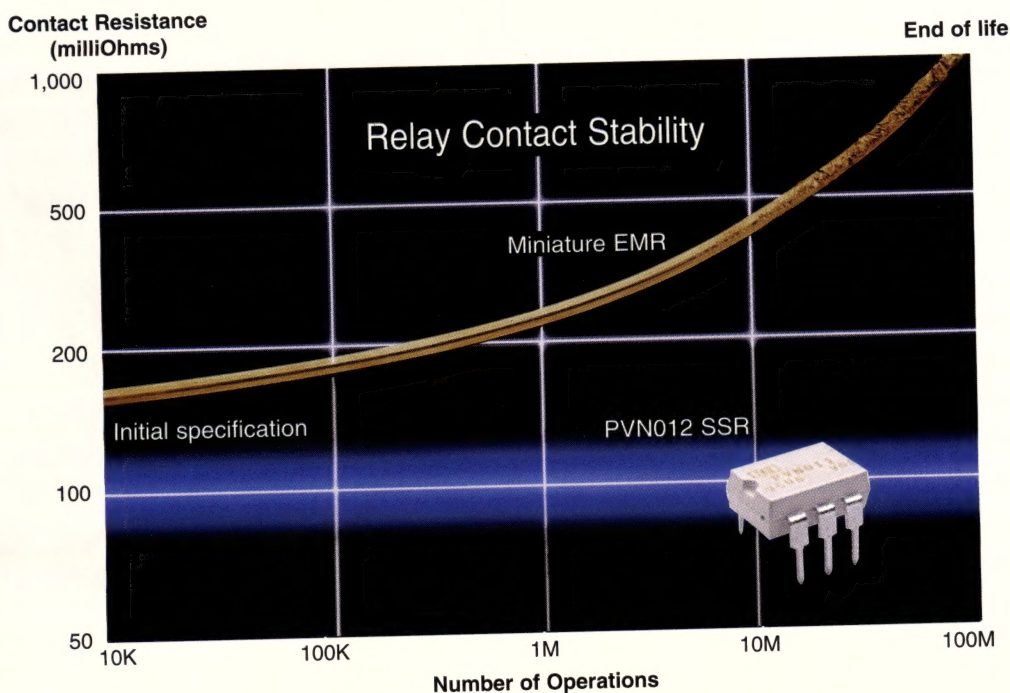
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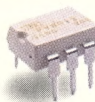
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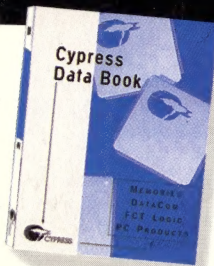
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